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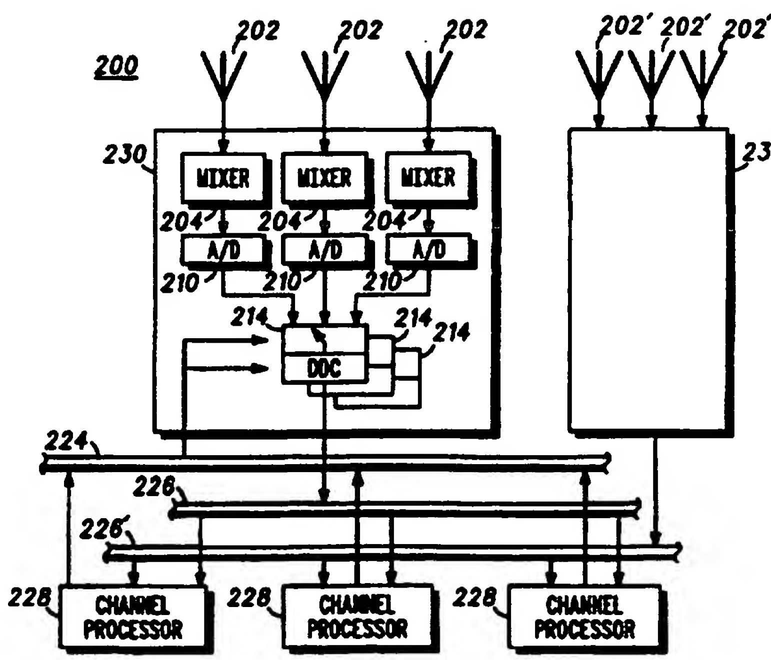
(54) Title: MULTIPLE ACCESS DIGITAL TRANSMITTER AND RECEIVER

(57) Abstract

A digital receiver (200) and a transmitter (300), wherein the digital receiver includes a plurality of antennas (202) for receiving uplink radio frequency signals; a plurality of analog to digital converters (210) for converting the received radio frequency signals into digital signals; a switched digital down converter (214) for down converting one of the digital signals to a baseband IF signal; and a channel processor (228) for recovering one of a plurality of communication channels contained within the baseband IF signal.



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MULTIPLE ACCESS DIGITAL TRANSMITTER AND RECEIVER

Field of the Invention

The present invention relates to communication system, and more particular to wideband transceivers for use in communication systems.

Background of the Invention

Transmitters and receivers for communication systems generally are designed such that they are tuned to transmit and receive one of a multiplicity of signals having widely varying bandwidths and which may fall within a particular frequency range. It will be appreciated by those skilled in the art that these transmitters and receivers radiate or intercept, respectively, electromagnetic radiation within a desired frequency band. The electromagnetic radiation can be output from or input to the transmitter or receiver, respectively, by several types of devices including an antenna, a wave guide, a coaxial cable and an optical fiber.

These communication system transmitters and receivers may be capable of transmitting and receiving a multiplicity of signals; however, such transmitters and receivers generally utilize circuitry which is duplicated for each respective signal to be transmitted or received which has a different frequency or bandwidth. This circuitry duplication is not an optimal multi-channel communication unit design architecture, because of the added cost and complexity associated with building complete independent transmitters and/or receivers for each communication channel.

An alternative transmitter and receiver architecture is possible which would be capable of transmitting and receiving signals having a desired multi-channel wide bandwidth. This alternative transmitter and receiver may utilize a digitizer (e.g., an analog-to-digital converter) which operates at a sufficiently high sampling rate to

ensure that the signal of the desired bandwidth can be digitized in accordance with the Nyquist criteria (e.g., digitizing at a sampling rate equal to at least twice the bandwidth to be digitized). Subsequently, the digitized signal preferably is pre- or post- processed using digital signal processing techniques to differentiate between the multiple channels within the digitized bandwidth.

With reference to FIG. 1, a prior wideband transceiver 100 is shown. Radio frequency (RF) signals are received at antenna 102 processed through RF converter 104 and digitized by analog-to-digital converter 106. The digitized signals are processed through a discrete fourier transform (DFT) 108, a channel processor 110 and from channel processors 110 to a cellular network and a public switched telephone network (PSTN). In a transmit mode, signals received from the cellular network are processed through channel processors 110, inverse discrete fourier transform (IDFT) 114 and digital-to-analog converter 116. Analog signals from digital-to-analog converter 116 are then up converted in RF up converter 118 and radiated from antenna 120.

A disadvantage of this alternative type of communication unit is that the digital processing portion of the communication unit must have a sufficiently high sampling rate to ensure that the Nyquist criteria is met for the maximum bandwidth of the received electromagnetic radiation which is equal to the sum of the individual communication channels which form the composite received electromagnetic radiation bandwidth. If the composite bandwidth signal is sufficiently wide, the digital processing portion of the communication unit is very costly and consumes a considerable amount of power. Additionally, the channels produced by a DFT or IDFT filtering technique must typically be adjacent to each other.

A need exists for a transmitter and a receiver, like the one which is described above, which is capable of transmitting and receiving a multiplicity of signals within corresponding channels with the same transmitter or receiver circuitry. However, this transmitter and

receiver circuitry preferably should reduce communication unit design constraints associated with the above transceiver architecture. If such a transmitter and receiver architecture could be developed, then it would be ideally suited for cellular radiotelephone communication systems. Cellular base stations typically need to transmit and receive multiple channels within a wide frequency bandwidth (e.g., 824 megahertz to 894 megahertz). In addition, commercial pressures on cellular infrastructure and subscriber equipment manufacturers are prompting these manufacturers to find ways to reduce the cost of communication units. Similarly, such a multi-channel transmitter and receiver architecture would be well suited for personal communication systems (PCS) which will have smaller service regions (than their counterpart cellular service regions) for each base station and as such a corresponding larger number of base stations will be required to cover a given geographic region. Operators which purchase base stations ideally would like to have a less complex and reduced cost unit to install throughout their licensed service regions.

An additional advantage may be gained by cellular and PCS manufacturers as the result of designing multi-channel communication units which share the same analog signal processing portion. Traditional communication units are designed to operate under a single information signal coding and channelization standard. In contrast, these multi-channel communication units include a digital signal processing portion which may be reprogrammed, at will, through software during the manufacturing process or in the field after installation such that these multi-channel communication units may operate in accordance with any one of several information signal coding and channelization standards.

Another disadvantage of traditional communication system design is that the hardware associated with the communication system is typically dedicated to a single access method (i.e., advanced mobile phone service (AMPS), narrowband advanced mobile phone service

(NAMPS), United States digital cellular (USDC), personal digital cellular (PDC) and the like communication access methods). In order to provide multiple access, i.e., access to the communication system through any of the access methods, significant hardware duplication, at considerable cost, is required. Therefore, there is a need for a communication system which provides for multiple access while not significantly increasing the amount of required hardware, and hence associated cost.

Digital signal processing is evolving as the preferred implementation in many signal processing applications. The advent of improved, higher speed and lower cost digital signal processors (DSPs) and other digital circuit elements coupled with increased flexibility and accuracy of digital circuits is driving a move to converting a number of signal processing applications from the analog forum to the digital forum. Digital signal processing, while offering the above mentioned advantages and other advantages, does not come without some drawbacks. For example, some applications, particularly in the field of radio frequency (RF) communications, are inherently analog. Signal processing for RF applications often require converting an analog signal, for example an RF or intermediate frequency (IF) signal, to a digital signal and likewise converting digital signals to analog signals. An example of such an application is in wideband digital transceivers such as shown and described in commonly assigned United States Patent Application Serial No. 08/366,283, the disclosure of which is hereby expressly incorporated herein by reference.

In many digital processing applications, including those accomplished in a wideband digital transceiver, the precision of a signal must be converted from a high level of precision to a lower level of precision. For example, a signal represented as 32 bits of information may have to be reduced to a signal represented as 16 bits of information. This is due to the limited capabilities of certain digital

processing elements such as, for example, digital-to-analog converters (DACs). In making such a conversion, however, there is a loss of information. One will appreciate in the above example that 32 bits can represent more information than 16 bits at a given data rate. The result of this loss of information is quantization noise.

Often the noise is distributed over the entire Nyquist bandwidth and the noise power per Hertz is negligible. However, frequently the noise appears at discreet frequencies, like second and third harmonics of the signal, which pose significant problems.

To overcome the problem of noise dwelling at particular frequencies, it has been proposed to introduce psuedorandom noise to the signal, often referred to as dithering. A number of dithering techniques are taught in U.S. Patents Nos. 4,901,265, 4,951,237, 5,073,869, 5,228,054 and 5,291,428. A major disadvantage of dithering is the requirement of having to provide pseudorandom noise generator circuitry which is often complex making the application implementation intensive and costly.

Therefore, a need exists for a method and apparatus for reducing quantization noise without significantly increasing the cost and complexity of the digital signal processing circuit.

There are numerous advantages to implementing a radio communication system using digital techniques. Notably, there is enhanced system capacity, reduced noise, and reduced hardware and associated power consumption. Fundamental to the digital radio communication system is the requirement that the received analog radio signal be digitized. The well known Nyquist criteria provides that such digitization is accomplished with minimal error at about twice the bandwidth of the analog signal. In United States Patent No. 5,251,218 a methodology typical of the prior art is disclosed for digitizing an analog radio frequency signal in accordance with this principle. It will be appreciated, however, where the radio signal occupies a large bandwidth, ADCs capable of operation at very high

sampling rates are required. Such devices, to the extent they are available, are expensive and often suffer reduced performance, i.e., have significant distortion and increased power consumption when operated at high sampling rates.

The spectrum allocated to radio communication systems is typically large with respect to the requirements for digitizing. In some radio communication systems, however, although the desired signal occupies a large bandwidth, not all of the bandwidth is occupied by signals of interest. In cellular radio telephone communication systems, for example, the communication bandwidth is not contiguous. The cellular A-band, for example, is allocated a bandwidth of 12.5 megahertz (MHz). Spectrally, however, the entire A-band covers 22.5 MHz of bandwidth in two discontinuous portions. In order to digitize the A-band, one would need an ADC capable of operating, according to Nyquist criteria, at least at 45 MHz or 45 million samples per second (Ms/s), and more reliably at 56Ms/s. Splitting the signal into smaller segments allows the use of multiple ADCs at lower sampling rates. Using multiple ADCs has the disadvantage of requiring more hardware. Furthermore, clock frequency and higher order harmonics thereof inevitably fall into the frequency band of the signal being digitized. Still another disadvantage is the amount of digital data handling required to filter, interpolate, compensate for band overlap and sum the resulting multiple digital signals.

Therefore, there is a need for a device for digitizing wideband frequency band signals which is does not require high sampling rates, and does not significantly increase the amount of hardware required for the communication system.

The many advantages and features of the present invention will be appreciated from the following detailed description of several preferred embodiments of the invention with reference to the attached drawings in which:

Brief Description of the Drawings

FIG. 1 is a block diagram of a prior art multi-channel transceiver;

FIG. 2 is a block diagram representation of a multi-channel receiver in accordance with a preferred embodiment of the present invention;

FIG. 3 is a block diagram representation of a multi-channel transmitter in accordance with a preferred embodiment of the present invention;

FIG. 4 is a block diagram representation of a multi-channel transceiver in accordance with a preferred embodiment of the present invention;

FIG. 5 is a block diagram representation of the multi-channel receiver shown in FIG. 2 and modified to provide per-channel scanning in accordance with another preferred embodiment of the present invention;

FIG. 6 is a block diagram representation of a multi-channel transceiver in accordance with another preferred embodiment of the present invention;

FIG. 7 is a block diagram representation of a multi-channel transceiver in accordance with another preferred embodiment of the present invention;

FIG. 8 is a block diagram representation of data routing in a multi-channel transceiver in accordance with a preferred embodiment of the present invention;

FIG. 9 is a block diagram representation of data routing in a multi-channel transceiver in accordance with another preferred embodiment of the present invention;

FIG. 10 is a block diagram representation of data routing in a multi-channel transceiver in accordance with another preferred embodiment of the present invention;

FIG. 11 is a block diagram representation of a digital converter module for the multi-channel transmitter of FIG. 5 and further in accordance with a preferred embodiment of the present invention;

FIG. 12 is a block diagram representation of a preferred embodiment of a digital down converter in accordance with the present invention;

FIG. 13 is a block diagram representation of a preferred embodiment of a digital up converter in accordance with the present invention;

FIG. 14 is a block diagram representation of an up converter adaptable to the digital up converter of the present invention;

FIG. 15 is a block diagram representation of a modulator adaptable to the digital up converter of the present invention;

FIG. 16 is a block diagram representation of a preferred embodiment up converter/modulator for the digital up converter of the present invention;

FIG. 17 is a block diagram representation of a preferred embodiment of a channel processor card in accordance with the present invention;

FIG. 18 is a block diagram representation of another preferred embodiment of a channel processor card in accordance with the present invention; and

FIG. 19 is a flowchart illustrating a scan procedure in accordance with a preferred embodiment of the present invention.

FIG. 20 is a block diagram representation of a quantization circuit in accordance with a preferred embodiment of the present invention.

FIG. 21 is a transfer function representation of a filter for use in the quantization circuit shown in FIG. 20.

FIG. 22 is graph spectrally illustrating quantization noise based upon truncation without the present invention.

FIG. 23 is graph spectrally illustrating the performance of the quantization circuit of FIG. 20.

FIG. 24 is a block diagram representation of a wideband frequency signal digitizer in accordance with a preferred embodiment of the present invention.

FIG. 25 is a block diagram representation of a wideband frequency signal digitizer in accordance with another preferred embodiment of the present invention.

FIG. 26 is a block diagram representation of a wideband frequency signal digitizer in accordance with another preferred embodiment of the present invention.

FIGs. 27A-27B spectrally illustrate the processing of a wideband frequency signal in accordance with a preferred embodiment of the present invention.

FIGs. 28-28H spectrally illustrate the processing of a wideband frequency signal in accordance with another preferred embodiment of the present invention.

FIG. 29 is a block diagram representation of a split frequency band digitizer in accordance with a preferred embodiment of the present invention.

FIG. 30A is a spectral representation of a split frequency band signal.

FIG 30B is a spectral representation of the split frequency band signal shown in FIG. 2A after translation according to a preferred embodiment of the present invention.

FIG 30C is a spectral representation of the split frequency band signal shown in FIG. 30B after converting to a digital signal in accordance with a preferred embodiment of the present invention.

FIG 31 is a flowchart illustrating a method of digitizing a split frequency band signal in accordance with a preferred embodiment of the present invention.

Detailed Description of a Preferred Embodiment

The present invention is directed to a wideband multi-channel transmitter and receiver (transceiver) which incorporates a high degree of flexibility and redundancy and which is particularly adaptable to the cellular or PCS communication systems. The transceiver provides support for multiple antennas for either sectorized cellular operation, diversity reception, redundancy or as preferred, a combination of all of these features with enhanced user capacity at reduced cost. The transceiver of the present invention accomplishes these and many other features through a practical architecture which enhances performance through incorporation of substantial digital processing and dynamic equipment sharing (DES).

The present invention further provides for multiple access without significant hardware duplication. A transceiver according to the present invention incorporates programmable digital down converters (DDCs) and programmable digital up converters (DUCs). That is, each of the DUCs and DDCs may be programmed to provide varying decimation/interpolation ratios to accommodate access methods with varying signal formats and bandwidths. However, the programmability of the DUC does not entirely provide for multiple access. Therefore, the DUC of the present invention also incorporates a unique hardware structure which provides both frequency modulation (FM) as well as quadrature (I and Q) up conversion without significant hardware duplication and associated cost.

With reference to FIG. 4, a transceiver 400 according to a preferred embodiment of the present invention is shown. For ease of discussion, preferred embodiments of wideband multi-channel digital receiver and transmitter portions, 200 and 300, respectively, of transceiver 400 are discussed. Furthermore, to present a preferred implementation of the present invention, a transceiver operable in the cellular radio frequency (RF) band is presented. It should be understood, however, that the present invention may be easily adapted to service any RF communication band including, for example, the PCS and the like bands.

With reference then to FIG. 2, a wideband multi-channel digital receiver portion (receiver) 200 in accordance with a preferred embodiment of the present invention is shown. The receiver 200 includes a plurality of antennas 202 (individually antennas 1,3,...,n-1) which are coupled, respectively, to a plurality of radio-frequency mixers 204 for converting RF signals received at antennas 202 to intermediate frequency (IF) signals. It should be appreciated that the mixers 204 contain the appropriate signal processing elements at least including filters, amplifiers, and oscillators for pre-conditioning the received RF signals, isolating the particular RF band of interest and mixing the RF signals to the desired IF signals.

The IF signals are then communicated to a plurality of analog-to-digital converters (ADCs) 210 where the entire band of interest is digitized. One past disadvantage of prior wideband receivers was the requirement that the ADC, to completely and accurately digitize the entire band, operate at a very high sampling rate. For example, the cellular A and B bands occupy 25 megahertz (MHz) of RF spectrum. In accordance with the well known Nyquist criteria, to accurately digitize the entire cellular bands with a single ADC would require a device capable of operating at a sampling rate of more than 50 MHz (or 50 million samples per second, 50 Ms/s). Such devices are becoming more common and it is contemplated within the scope of the present invention to utilize the latest ADC technology. However,

commonly assigned United States Patent Applications filed of even date herewith and entitled "Split Frequency Band Signal Digitizer and Method" by Smith et al. and "Wideband Frequency Signal Digitizer and Method" by Elder, the disclosures of which are hereby expressly incorporated herein by reference, disclose devices and methods for completely and accurately digitizing a wideband frequency signal using ADCs operating at lower sampling rates. The ADCs 210 digitize the IF signals thereby producing digital signals. These digital signals are then communicated to digital down converters (DDCs) 214.

The DDC 214 of the preferred embodiment, seen more clearly in FIG. 12, includes a switch 1216 which allows DDC 214 to select IF signals from any one of the plurality of antennas 202. Based on the state of switch 1216, the DDC 214 accepts a high speed stream of digital words (e.g. approximately 60 MHz) from the ADC 210 associated with the selected antenna, in the preferred embodiment via a backplane interconnect 1108, FIG. 11. The DDC 214 is operable to select a particular frequency (in the digital domain), to provide decimation (rate reduction) and to filter the signal to a bandwidth associated with channels of the communication system. With particular reference to FIG. 12, each DDC 214 contains a numerically controlled oscillator (NCO) 1218 and a complex multiplier 1220 to perform a down conversion on the digital word stream. Note, this is a second down conversion since a first down conversion was performed on the received analog signal by mixers 204. The result of the down conversion and complex multiplication is a data stream in quadrature, i.e., having in-phase, I, and quadrature, Q, components, which has been spectrally translated to a center frequency of zero hertz (baseband or zero IF). The I,Q components of the data stream are communicated to a pair of decimation filters 1222, respectively, to reduce the bandwidth and the data rate to a suitable rate for the particular communication system air interface (common air interface or CAI) being processed. In the preferred embodiment, the data rate output of the decimation filters is about 2.5 times the desired

bandwidth of the CAI. It should be understood that the desired bandwidth may change the preferred decimation filters 1222 output rate. The decimated data stream is then low pass filtered to remove any undesirable alias components through digital filters 1224. Decimation filters 1222 and digital filters 1224 provide rough selectivity, final selectivity is accomplished within the channel processors 228 in a known manner.

Observed in FIG. 2, a plurality of DDCs 214 are provided in the preferred embodiment and each are interconnected to ADCs 210. Each of the DDCs 214 can select one of the plurality of ADCs 210/antennas 202 from which to receive a high speed digital word stream via backplane 1106. The outputs of the DDCs 214, a low speed data stream (e.g. approximately 10 MHz, baseband signal), are connected to a time domain multiplex (TDM) bus 226 for communication to a plurality of channel processors 228 via output formatter 1232. By placing the outputs of the DDCs on TDM bus 226, it is possible to have any one of the channel processors 228 select any one of the DDCs 214 for receiving a baseband signal. In the event of a failure of a channel processor 228 or a DDC 214, the channel processors 228 would be operable, via the control bus 224 and control bus interface 1234, to interconnect available channel processors to available DDCs with appropriate contention/arbitration processing to prevent two channel processors from attempting to access the same DDC. In the preferred embodiment, however, the DDCs 214 are allocated a dedicated time slot on TDM bus 226 for interconnection to a particular channel processor 228.

The channel processors 228 are operable to send control signals via the control bus 224 to the DDCs 214 for setting digital word stream processing parameters. That is, the channel processors 228 can instruct the DDCs 214 to select a down conversion frequency, a decimation rate and filter characteristics (e.g., bandwidth shape, etc.) for processing the digital data streams. It is understood that the NCO 1218, complex multiplier 1220, decimator 1222 and digital filter 1224

are responsive to numerical control to modify the signal processing parameters. This allows receiver 200 to receive communication signals conforming to a number of different air interface standards.

With continued reference to FIG. 2, the receiver of the present invention further provides a plurality of receiver banks (two shown and illustrated as 230 and 230'). Each of the receiver banks 230 and 230' include the elements described above prior to TDM bus 226 for receiving and processing a radio frequency signal. In order to provide diversity reception with the present invention, a pair of adjacent antennas, one from antennas 202 and one from antennas 202' (individually referenced as 2,4,..., n), each associated with receiver banks 230 and 230', respectively, are designated to service a sector of the communication system. The signals received at each antenna 202 and 202' are processed independently through receiver banks 230 and 230', respectively. The outputs of the receiver banks 230 and 230' are communicated respectively on TDM buses 226 and 226', although it is understood that a single bus may be used, to the channel processors 228, wherein the diversity reception is accomplished.

The channel processors 228 receive the baseband signals and perform the required baseband signal processing, selectivity to recover communication channels. This processing at least includes audio filtering in analog CAI communication systems, forward error correction in digital CAI communication systems, and receive signal strength indication (RSSI) in all communication systems. Each channel processor 228 recovers traffic channels independently. Furthermore, to provide diversity, each channel processor 228 is operable to listen to each of the pair of antennas assigned to a sector and to thereby receive and process two baseband signals, one per antenna. The channel processors 228 are further provided an interface 436, FIG. 4, to the communication network, for example in a cellular communication system to a base station controller or mobile switching center, via a suitable interconnect

With reference to FIG. 17 a preferred embodiment of a channel processor 228 is shown. As will be described, each of the channel processors is operable for both transmit and receive operations. In the preferred embodiment, each channel processor 228 is capable of servicing up to 8 communication channels of the communication system in both transmit and receive (4 channels in receive mode with diversity). The low speed baseband signal from TDM buses 226 or 226' are received respectively at input/output (I/O) ports 1740 and 1740' and are communicated to a pair of processors 1742 and 1742'. Associated with each processor 1742 and 1742', are digital signal processors (DSPs) 1744 and 1744' and memory 1746 and 1746'. Each processor 1742 and 1742' is operable to service four (4) communication channels. As can be seen in FIG. 17, in a preferred embodiment, the processors 1742 and 1742' are configured to listen to either one, or both as is required in the preferred diversity arrangement, of the receiver banks 230 or 230'. This structure, while also enabling diversity, provides redundancy. In the receive mode if one of the processors 1742 or 1742' fails, only diversity is lost as the other processor 1742 or 1742' is still available to process the uplink baseband signals from the other receiver bank. It should be appreciated that processors 1742 and 1742' can be implemented with appropriate diversity selection or diversity combining processing capability. Processors 1742 and 1742' are further in communication with control elements 1748 and 1748', respectively, for processing and communicating control information to the DDCs 214 via I/O ports 1740 and 1740' and the control bus 224 as described.

With continued reference to FIG. 17 and reference to FIG. 4, the transmitter portion 300 (transmitter) of transceiver 400 will be described. In a transmit mode, the channel processors 228 receive downlink communication signals from the communication system network (via interface 436 not shown in FIG. 17) for communication over a communication channel. These downlink signals can be, for example, control or signaling information intended for the entire cell (e.g., a page message) or a particular sector of a cell (e.g., a handoff

command) or downlink voice and/or data (e.g., a traffic channel). Within channel processors 228, processors 1742 and 1742' independently operate on the downlink signals to generate low speed baseband signals. In transmit mode, the channel processors 228 are capable of servicing eight (8) communication channels (either traffic channels, signaling channels or a combination thereof). If one of the processors 1742 or 1742' fails, the effect on the system is a loss of capacity, but not a loss of an entire sector or cell. Moreover, removing one of the plurality of channel processors 228 from the communication system results in the loss of only eight channels.

The processing of the baseband signals through the transmitter 300 is complementary to the processing completed in the receiver 200. The low speed baseband signals are communicated from the channel processors 228 via I/O ports 1740 or 1740' to TDM downlink busses 300 and 300', although a single bus may be used, and from there to a plurality of digital up converters (DUCs) 302. The DUCs 302 interpolate the baseband signals to a suitable data rate. The interpolation is required so that all baseband signals from the channel processors 228 are at the same rate allowing for summing the baseband signals at a central location. The interpolated baseband signals are then up converted to an appropriate IF signal such as quadrature phase shift keying (QPSK) differential quadrature phase shift keying (DQPSK), frequency modulation (FM) or amplitude modulation (AM) signals (with I,Q input, the modulation is accomplished within the channel processors 228). The baseband signals are now carrier modulated high speed baseband data signals offset from zero hertz. The amount of offset is controlled by the programming of the DUCs 302. The modulated baseband signals are communicated on a high speed backplane interconnect 304 to signal selectors 306. The signal selectors are operable to select sub-groups of the modulated baseband signals. The selected sub-groups are communication channels which are to be transmitted within a particular sector of the communication system. The selected sub-group of modulated baseband signals are then communicated to digital

summers 308 and summed. The summed signals, still at high speed, are then communicated, via backplane interconnect 1130 to digital-to-analog converters (DACs) 310 and are converted to IF analog signals. These IF analog signals are then up converted by up converters 314 to RF signals, amplified by amplifiers 418 (FIG. 4) and radiated from antennas 420 (FIG. 4).

In the preferred embodiment, to once again provide enhanced system reliability, a plurality of DACs 310 are provided with groups 311 of three DACs being arranged on RF shelves, one DAC associated with a shelf. The groups of DACs 311 convert three summed signals, received on separate signal busses 313 of backplane interconnect 1130, to analog signals. This provides for increased dynamic range over what could be achieved with a single DAC. This arrangement further provides redundancy since if any of the DACs fail, there are others available. The result is merely a decrease in system capacity and not a loss of an entire sector or cell. The outputs of a group of DACs 311 receiving signals for a sector of the communication system are then analog summed in summers 312, with the summed analog signal being communicated to up converters 314.

Similar to the receiver 200, the transmitter 300 is also arranged with a plurality of transmitter banks (two shown as 330 and 330'). The transmitter banks 330 and 330' include all of the equipment for the transmitter 300 between the channel processors 228 and the amplifiers 418. The output of the up converters 314, up converting summed analog signals for a sector of the communication system, for each transmitter bank 330 and 330' are then summed in RF summers 316. The summed RF signals are then communicated to amplifiers 418 and radiated on antennas 420. If an entire transmitter bank 330 or 330' fails, the effect is still only a loss of system capacity and not a loss of an entire portion of the communication system.

With reference to FIG. 13 a DUC 302 in accordance with a preferred embodiment of the present invention is shown. In the preferred embodiment, there is provided a plurality of DUCs 302

each of which includes an up converter/modulator 1340 which receives downlink baseband signals from busses 300 and 300' and control signals from control bus 224 via formater circuits 1341. The output of the up converter/modulator 1340 is then communicated to selector 306. In the preferred embodiment, selector 306 can take the form of banks of dual-input AND gates, one input of which is connected to one bit of the data word (i.e. the modulated baseband signal). With the control line held high (logical 1), the outputs will follow the transitions of the inputs. The output of selector 306 is then communicated to a digital summer bank 1308, which adds data from previous digital summers associated with other DUCs onto one of a plurality of signal paths 313. Each signal path, as indicated, is associated with a sector of the communication system and communicates the summed signals to DAC groups 311. If selector 306 is open, the output of selector 306 is zeros, and as an input to summer 1308 leaves the incoming signal unchanged. It should also be understood that scaling may be required on the input, the output or both of summers 1308 for scaling the summed digital signal within the dynamic range of the summers 1308. In this manner, the outputs of the DUCs, representing signals destined for particular sectors of the communication system can be summed into a single signal for conversion to an analog signal. Or, as is accomplished in the preferred embodiment, may be further collected in sets and converted to analog signals by multiple DACs for enhancing the dynamic range and providing redundancy.

With reference to FIG. 14, an up converter 1400 for I,Q modulation in accordance with the present invention is shown. The up converter 1400 includes first and second interpolation filters 1402 and 1404 (e.g., finite impulse response (FIR) filters) for interpolating the I,Q portions of the baseband signal, respectively. The interpolated I,Q portions of the baseband signal are up converted in mixers 1406 and 1408, receiving input from numerically controlled oscillator 1410. Numerically controlled oscillator (NCO) 1410 receives as an input the product of the up conversion frequency, ω_o, and the inverse sample

rate, τ, which is a fixed phase increment dependent on the up conversion frequency. This product is supplied to a phase accumulator 1412 within NCO 1410. The output of phase accumulator 1412 is a sample phase, Φ, which is communicated to sine and cosine generators 1414 and 1416, respectively, for generating the up conversion signals. The up converted I,Q portions of the baseband signal are then summed in summer 1418 providing the modulated IF signal output of up converter 1400.

In FIG. 15, a modulator 1500 for R,Θ modulation, direct modulation of the phase, is shown. Modulator 1500 provides a simplified way of generating FM over up converter 1400. The baseband signal is communicated to interpolation filter 1502(e.g., a FIR filter) which is then scaled by $k\tau$ in scaler 1504. The interpolated and scaled baseband signal is then summed in summer 1506 with the fixed phase increment $\omega_0\tau$ in a numerically controlled oscillator/modulator (NCOM) 1508. This sum is then communicated to a phase accumulator 1510 which outputs a sample phase, Φ, which in turn is communicated to a sinusoid generator 1512 for generating the modulated IF signal output of modulator 1500.

The devices shown in FIGs. 14 and 15 are suitable for use in up converter/modulator 1340 of the present invention. However, the up converter 1400 is not efficient with respect to generating FM, while modulator 1500 does not provide I,Q up conversion. In FIG. 16, a preferred up converter/modulator 1340 is shown which provides both I,Q up conversion and FM modulation, and hence, provides for multiple access using various access methods without significantly increasing base station hardware and cost. Up converter/modulator 1340 provides I,Q up conversion for a single baseband signal or R,Θ modulation for two baseband signals.

The I,Q portions of the baseband signal or two R,Θ signals are input to up converter/modulator 1340 at ports 1602 and 1604, respectively. Signal selectors 1606 and 1608 are provided and select

between the I,Q or R,Θ signals based upon the mode of operation of up converter/modulator 1340.

With respect to processing of an I,Q signal, the I portion of the signal is communicated from selector 1606 to interpolation filter, (e.g., an FIR filter) 1610. The interpolated I signal is then communicated to mixer 1612 where it is up converted by a sinusoid from cosine generator 1614. Cosine generator 1614 receives an input sample phase Φ from phase accumulator 1616. A selector 1618 is provided and selects a zero input for I,Q up conversion. The output of selector 1618 is scaled by $k\tau$ in scaler 1620 yielding a zero output which is added to $\omega_O\tau$ in adder 1622. This sum, which is $\omega_O\tau$ in the I,Q up conversion case, is input to phase accumulator 1616 to produce the sample phase output, Φ.

Processing of the Q portion of the signal is similar. The Q signal is selected by selector 1608 and communicated to interpolation filter (e.g., an FIR filter) 1626. The interpolated Q signal is then communicated to mixer 1628 where it is up converted by a sinusoid from sine generator 1630. Sine generator 1630 receives an input from selector 1632 which selects the sample phase, Φ, generated by phase accumulator 1616 in the I,Q case. The up converted I,Q signals are then summed in summer 1634 as the up converted/modulated output of up converter/modulator 1340 in the I,Q mode.

In R,Θ processing, the selectors 1606 and 1608 select two separate R,Θ signals. For R,Θ processing, up converter/modulator 340 is operable to process two R,Θ signals simultaneously. The first signal, R,Θ-1 is interpolated and filtered in interpolation filter 1610. In the R,Θ case, selector 1618 selects the interpolated R,Θ–1 signal which is scaled by $k\tau$ in scaler 1620 and added to $\omega_O\tau$ in adder 1622. The output of adder 1622 is then communicated to phase accumulator 1616 which produces a sample phase, Φ which is input to cosine generator 1614. The output of cosine generator 1614 is one of two modulated IF signal outputs of up converter/modulator 1340 in R,Θ processing mode.

The second R,Θ signal, R,Θ-2, is selected by selector 1608 and is communicated to interpolation filter 1626. The interpolated R,Θ-2 signal is then communicated to scaler 1636 where it is scaled by $k\tau$. The scaled signal is then summed with $\omega_O\tau$ in adder 1638. The output of adder 1638 is input to phase accumulator 1640 which produces an output sample phase, Φ, which is selected by selector 1632 and communicated to sine generator 1630. The output of sine generator 1630 is the second of two modulated IF signal outputs of up converter/modulator 1340 in R,Θ processing mode.

It will be appreciated that the value $\omega_O\tau$ communicated to adders 1622 and 1638 may be unique to provide the proper phase output associated with either cosine generator 1614 or sine generator 1630. Furthermore, the values of $\omega_O\tau$ may be programmable under control of the channel processors 228, for example, to select a particular carrier frequency output from cosine generator 1614 or sine generator 1630. Likewise, the scaler value $k\tau$ may be similarly programmable to select frequency deviation.

Having now described separately the receiver 200 and transmitter 300 portions of transceiver 400, transceiver 400 will be described in more detail with reference to FIG. 4. Transceiver 400 is structured in a pair of transceiver banks 402 and 404. Each bank is identical and includes a plurality of RF processing shelves 406. Each RF processing shelf 406 houses a RF mixer 408 and an ADC 410 which are coupled to receive and digitize a signal from antenna 412. RF processing shelf 406 further includes three DACs 414, the outputs of which are summed by summer 416 and communicated to RF up converter 418. The output of RF up converter 417 is further communicated to an RF summer 419 for summing with a corresponding output from transceiver bank 404. The summed RF signal is then communicated to amplifier 418 where it is amplified before being radiated from antenna 420.

Received signals from ADC 410 are interconnected to a plurality of digital converter modules (DCMs) 426 via receive busses 428.

Similarly, transmit signals are communicated from DCMs 426 to DACs 414 via transmit busses 430. As will be appreciated, receive busses 428 and transmit busses 430 are high speed data buses implemented into a backplane architecture within RF frame 432. In the preferred embodiment, communication over the backplane is at approximately 60 MHz, however, the close physical relationship of the elements allows for such high speed communication without significant errors in the high speed data signal.

With reference to FIG. 11 a preferred embodiment of a DCM 426 is illustrated. DCM 426 includes a plurality of DDC application specific integrated circuits (ASICs) 1102 and a plurality of DUC ASICs 1104 for providing receive and transmit signal processing. Receive signals are communicated from antennas 412 via a receive backplane interconnect 1108, backplane receiver 1106 and buffer/driver bank 1107 to DDC ASICs 1102 over communication links 1110. In the preferred embodiment, DCM 426 includes ten DDC ASICs 1102 each DDC ASIC 1102 having implemented therein three individual DDCs, as described above. In the preferred embodiment, eight of the DDC ASICs 1102 provide communication channel functions while two of the DDC ASICs 1102 provide scanning functions. The outputs of DDC ASICs 1102 are communicated via links 1112 and backplane formater 1114 and backplane drivers 1116 to the backplane interconnect 1118. From backplane interconnect 1118, receive signals are communicated to an interface media 450 (FIG. 4) for communication to a plurality of channel processors 448 arranged in groups in processor shelves 446.

In transmit mode, transmit signals are communicated from channel processors 448 over the interface media 450 and backplane interconnect 1118 through transmit backplane receivers 1120 to a plurality of DUC ASICs 1104 via selector/formater 1124. Each of the DUC ASICs 1104 contain four individual DUCs, the DUCs as described above, for processing four communication channels in R,Θ mode or two communication channels in I,Q mode. The outputs of

DUC ASICs 1104 are communicated via links 1126 to transmit backplane drivers 1128 and backplane interconnect 1130 for communication to the DACs 414

It should be understood that suitable provision is made for providing clock signals to the elements of DCM 426 as generally indicated as 460.

With respect to interface media 450, located between the DCMs 426 and the channel processors 448, interface media 450 may be any suitable communication media. For example, interface media may be a microwave link, TDM span or fiber optic link. Such an arrangement would allow for channel processors 448 to be substantially remotely located with respect to the DCMs 426 and the RF processing shelves 406. Hence, the channel processing functions could be accomplished centrally, while the transceiver functions are accomplished at a communication cell site. This arrangement simplifies construction of communication cell sites as a substantial portion of the communication equipment can be remotely located from the actual communication cell site. The result is a savings to the operator by way of physical space required for equipment and in more centralized operation and maintenance activity.

As shown in FIG. 4, transceiver 400 includes three DCMs 426, with a capability of twelve communication channels per DCM 426. This arrangement provides system reliability. Should a DCM 426 fail, the system loses only a portion of the available communication channels. Moreover, DCMs may be modified to provide multiple air interface capability. That is the DDCs and DUCs on the DCMs may be individually programmed for particular air interfaces. Hence, transceiver 400 provides multiple air interface capability.

As appreciated from the foregoing, there are numerous advantages to the structure of transceiver 400. With reference to FIG. 5 a receiver 500 of transceiver 400 is shown which is very similar to the receiver 200 shown in FIG. 2. The plurality of DDCs 214 and the interconnecting TDM bus 226 have been removed for clarity only,

and it should be understood that receiver 500 includes these elements. Receiver 500 includes an additional DDC 502 interconnected as before via a selector 504 to ADCs 506 for receiving uplink digital signals from antennas 508/mixers 509 and for communicating data signals to channel processors 510 via data bus 514. During operation, it may be necessary for a channel processor 510 to survey other antennas, antennas other than an antenna it is presently processing a communication channel for, to determine if it is communicating over the best antenna in the communication cell. That is, if an antenna servicing another sector of the communication cell provides better communication quality, the communication link should be reestablished on that antenna. To determine the availability of such antennas providing better communication quality, the channel processor scans each sector of the communication cell. In the present invention, this is accomplished by having the channel processor 510 seize DDC 502 and program it, via the control bus 512, to receive communications from each of the antennas in the communication cell. The information received, for example received signal strength indications (RSSI) and the like, are evaluated by channel processors 510 to determine if a better antenna exists. The processing in DDC 502 is identical to the processing accomplished in DDCs 214, with the exception that DDC 502, under instruction of channel processor 510, receives signals from a plurality of the antennas in the communication cell as opposed to a single antenna servicing an active communication channel

FIG. 19 illustrates a method 1900-1926 of accomplishing this per-channel scanning feature. The method enters at bubble 1900 and proceeds to step 1902 where a timer is set. The channel processor then checks if DDC 302 is idle, decision step 1904, i.e., not presently performing a scan for another channel processor; and, if it is idle, checks to see if the control bus 312 is also idle, decision step 1906. If it is, the timer is stopped 1908 and channel processor 310 seizes the control bus 312, 1909. If channel processor 310 is unable to seize the control bus 312, 1912, then the method loops back to step 1902. If

either the DDC 302 or the control bus 312 are not idle, then a time out check is made, 1910, if time out has not been reached, the method loops back to check if the DDC has become available. If a time out has been reached, an error is reported, 1920, i.e., channel processor 310 was unable to complete a desired scan.

If the control bus 312 is successfully seized, 1912, channel processor programs DDC 302 for the scan function, 1914. If, however, DDC 302 has become active 1916, the programming is aborted and an error is reported, 1920. Otherwise, the DDC 302 accepts the programming and begins collecting samples, 1918, from the various antennas 308. When all the samples are collected, 1922, the DDC is programmed to an idle state, 1924, and the method ends 1926.

Another feature of transceiver 400 is an ability to provide signaling to particular sectors or to all sectors of a communication cell. With reference once again to FIGs. 3 and 13, the outputs of up converter/modulators 1340 are communicated to selectors 306 which are operable to select outputs from the plurality of up converter/modulators 1340 which are to be directed to a particular sector of the communication cell. As illustrated in FIG. 3, for a three sector communication cell, three data paths 313 are provided corresponding to the three sectors of the communication cell, and the function of selectors 306 is to sum the output of up converters/modulators 1340 onto one of these three data paths. In this manner, the downlink signals from up converters/modulators 1340 are communicated to an appropriate sector of the communication cell.

Selector 306, however, is further operable to apply the output of an up converter/modulator 1340 to all of the signal paths 313. In this case, the downlink signals from the up converter/modulator 1340 is communicated to all sectors of the communication cell simultaneously. Hence, an omni like signaling channel, through simulcast, is created by designating an up converter/modulator as a signaling channel and programming selector 306 to communicate the downlink signals from

this up converter/modulator to all sectors of the communication cell. Moreover, it should be appreciated that signaling to particular sectors may be accomplished by reprogramming selector 306 to communicate the downlink signals from a signaling up converter/modulator 1340 to one or more sectors of the communication cell.

With reference to FIG. 6, a transceiver 600 is shown which, while containing the functional elements described with respect to transceiver 400, provides a different architectural arrangement. Transceiver 600 advantageously provides uplink digital down conversion and corresponding downlink digital up conversion within the channel processors. The channel processors are then interconnected to the RF hardware via a high speed link.

In a receive mode, RF signals are received at antennas 602 (individually number 1, 2, ..., n) and are communicated to associated receive RF processing shelves 604. Each receive RF shelf 604 contains an RF down converter 606 and an analog to digital converter 608. The outputs of the receive RF shelves 604 are high speed digital data streams which are communicated via an uplink bus 610 to a plurality of channel processors 612. The uplink bus 610 is a suitable high speed bus, such as a fiber optic bus or the like. The channel processors 612 include a selector for selecting one of the antennas from which to receive a data stream and a DDC and other baseband processing components 613 for selecting and processing a data stream from one of the antennas to recover a communication channel. The communication channel is then communicated via a suitable interconnect to the cellular network and PSTN.

In a transmit mode, downlink signals are received by the channel processors 612 from the cellular network and PSTN. The channel processors include up converter/modulators 615 for up converting and modulating the downlink signals prior to communicating a downlink data stream to transmit RF processing shelves 614 over transmit bus 616. In should be understood that transmit bus 616 is also a suitable high speed bus. Transmit RF processing shelves 614 include the

digital summers 618, DACs 620 and RF up converters 622 for processing the downlink data streams into RF analog signals. The RF analog signals are then communicated via an analog transmit bus 624 to power amplifier 626 and antennas 628 where the RF analog signals are radiated.

With reference to FIG. 7, a transceiver 700 is shown which, while also containing the functional elements described with respect to transceiver 400, provides still another architectural arrangement. Transceiver 700 is described for a single sector of a sectorized communication system. It should be appreciated that transceiver 700 is easily modified to service a plurality of sectors.

In a receive mode, RF signals are received by antennas 702 and communicated to receive RF processing shelves 704. Receive RF processing shelves 704 each contain an RF down converter 703 and an ADC 705. The output of receive RF processing shelves 704 is a high speed data stream which is communicated via high speed backplane 706 to a plurality of DDCs 708. DDCs 708 operate as previously described to select the high speed data streams and to down convert the data streams. The outputs of DDCs 708 are low speed data streams which are communicated on busses 710 and 712 to channel processors 714. Channel processors 714 operate as previously described to process a communication channel and to communicate the communication channel to the cellular network and PSTN via a channel bus 716 and network interfaces 718. The DDCs 708 of transceiver 700 may also be advantageously located on a channel processor shelf with an appropriate high speed backplane interconnect.

In a transmit mode, downlink signals are communicated from the cellular network and PSTN via interfaces 718 and channel bus 716 to the channel processors 714. Channel processors 714 include DUCs and DACs for up converting and digitizing the downlink signals to analog IF signals. The analog IF signals are communicated via coaxial cable interconnects 722, or other suitable interconnection media, to a transmit matrix 724 where the downlink signals are combined with

other downlink analog IF signals. The combined analog IF signals are then communicated, via coaxial interconnects 726, to RF up converters 728. RF up converters 728 convert the IF signals to RF signals. The RF signals from up converters 728 are RF summed in summer 730 and are then communicated to power amplifiers and transmit antennas (not shown).

As will be appreciated from transceiver 700, the high speed data processing, i.e., the digital up conversion, on the downlink signals is advantageously accomplished within the channel processors 714. A preferred embodiment of a channel processor 714 is shown in FIG. 18. Channel processor 714 is similar in most aspects to channel processor 228 shown in FIG. 17 with like elements bearing like reference numeral. Channel processor 714 includes, in addition to these element, DUCs 1802 which are coupled to receive downlink signals from processors 1742, 1742'. DUCs 1802 up convert the downlink signals which are communicated to DACs 1806 where the downlink signals are converted to analog IF signals. The analog IF signals are then communicated, via ports 1740, 1740', to the transmit matrix 724.

With reference to FIGs. 8, 9 and 10 further arrangements for interconnecting the elements of transceiver 400 are shown. To avoid the loss of an entire cell due to the failure of a single component, daisy chain interconnection of components is avoided. As seen in FIG. 8, and for example in the downlink arrangement, selectors 800 are provided in the DCMs 802 prior to DUCs 804 and DAC 806. Direct data links 808 are provided from DUCs 804 to selectors 800 from DCM 802 to DCM 802 and finally to DAC 806. Bypass data links 810 are also provided tapping into direct data links 808. In operation, if one or more DCMs 802 fails, selectors 800 are operable to activate the appropriate bypass data links 810 to bypass the failed DCM 802 and to allow continued communication of signals to amplifier 812 and transmit antenna 814. It should be understood that the uplink elements

can be similarly connected to provide a fault tolerant receive portion of the transceiver.

FIG. 9 shows an alternate arrangement. In FIG. 9, channel processors 920 are interconnected via a TDM bus 922 to DCMs 902. DCMs are interconnected as described in FIG. 8, selectors 900 associated with each DCM 902 are not shown, it being understood that selectors may easily be implemented directly in the DCMs 902. By pass links 924 interconnecting the channel processors 920 directly to an associated DCM, and into an additional selector (not shown) within DCMs 902. In the event of the failure of a channel processor 920 bringing down TDM bus 922 or a failure of TDM bus 922 itself, the selectors within the DCMs 902 can activate the appropriate bypass link 924 to allow continued communication of signals to DAC 906, amplifier 912 and transmit antenna 914.

FIG. 10 shows still another alternate arrangement. Again, DCMs 1002 are interconnected as described in FIG. 8. In FIG. 10 direct links 1030 interconnect channel processors 820 in a daisy chain fashion, the output of each channel processor 1020 being summed in summers 1032 and then communicated to DCMs 1002 on a TDM bus 1034. By pass links 1036 forming a second bus, are provided as are selectors 1038 in a fashion similar to that shown for DCMs 802 in FIG. 8. In the event of a failure of any one of the channel processors, the signals from the remaining channel processors 1020 can be routed around the failed channel processors in the same manner as described for the DCMs 802, above to selector 1000, DAC, 1006, amplifier 1012 and antenna 1014.

According to the present invention, a feedback signal is provided to the input of a quantization circuit to reduce quantization noise. The feedback signal is generated as a filtered difference between a sample of the N bit signal and a time coincident sample of a M bit quantized signal, where M < N. The feedback signal is subtracted from the input signal prior to quantization thereby introducing out of band

noise into the input signal for reducing in band noise in the quantized signal.

With reference to FIG. 20, a N bit to M bit, where M < N, quantization circuit 2000 in accordance with the present invention is shown. A N bit signal **X**, is coupled to a summer 2002 where a N bit feedback signal **W** is subtracted. The resulting signal **X'** is then sampled in a N bit latch 2004 and concomitantly quantized in a M bit hard quantizer 2006. Hard quantizer truncates the N - M LSBs of signal **X'**, effectively setting the M - N LSBs to a value of zero. A N bit error signal **E**, is generated in summer 2008 as the difference between the M most signification bits (MSBs) of the N bit sample of **X'** contained in latch 2004 and the M bit quantized sample contained in hard quantizer 2006. The LSBs of the N bit sample of **X'** pass unchanged. Error signal **E** is filtered through filter 2010 creating N bit feedback signal **W**. It should be appreciated, however, that any M bits of signal **X'** may retained in hard quantizer 2006 depending on the particular application.

Further shown in FIG. 20 is a 12 bit DAC 2012 for converting hard quantizer output signal **Y** to an analog signal. It should be understood, however, that quantization circuit 2000 of the present invention is useful in any digital signal processing application requiring a conversion from a high precision information signal to a lower precision information signal where it is critical to avoid introduction of quantization noise.

Filter 2010 is chosen to pass only components of error signal **E** which are out of band with respect to input signal **X**. In the preferred embodiment, filter 2010 is a low pass filter which substantially maintains the noise components introduced into signal **X'** by feedback signal **W** at low frequencies and away from the band of interest. This is illustrated in FIGs. 22 and 23. As can seen in the FIG. 22, without the present invention, spurious noise components, illustrated at f_S, having signicant energy are present around the signal of interest illustrate at f_X. As can be seen in FIG. 23, while there is a substantial

amount of energy below a frequency f_{CO}, the cut off frequency of filter 2010, there is only a low level of noise which is substantially evenly distributed about the signal of interest at frequency f_X. In testing the present invention, a noise floor of (-93) dBc was observed about f_X as compare to (-72) dBc as may be typically expected from a 12 bit quantizer without the present invention. These data were generated referencing the analog signal output of DAC 2012.

Another feature of the quantization circuit 2000 is that when signal **X** is not present, or is substantially zero, there is no noise output. With prior art dithering techniques, psuedorandom noise is continuously input to the quantization circuit. When no input signal is present, the output signal of the quantization circuit is the pseudorandum noise. In the present invention, when input signal **X** is absent or substantially zero, the difference taken between the N bit sample of **X'** and the M bit quantized sample is substantially zero. Hence, the output of quantization circuit 2000 is zero when no input signal is present.

As described with respect to a preferred implementation of quantization circuit 2000, error signal **E** is a 16 bit signal. However, since it is the N - M LSBs which primarily contribute to error signal **E**, a N - M bit signal could be substituted. In such an implementation, the sign information of error signal **E** will be lost. Hence, it may be more desirable to implement a (N - M) + 1 bit error signal which retains the sign bit from signal **X'**. Such an implementation simplifies the data path for error signal **E** as well as reduces the size of filter 210.

With reference to FIG. 21, a transfer function for a preferred implementation of filter 2010 is shown. As can be seen in FIG. 21, filter 2010 is a 3 real pole filter which can be implemented using three full adders 2302, 2304 and 2306 and one delay element 2308. In the preferred embodiment of the present invention, the poles of filter 2010 are selected to be at 15/16 which allows for the simplified implementation shown in FIG. 21. As can be seen, this

implementation advantageously eliminates the need for multipliers which allows a simplified implementation of filter 2010 in an application specific integrated circuit (ASIC). Filter 2010 further includes an overall gain factor, in the preferred embodiment approximately 100 dB. Gain is provided at each stage of filter 2010 which enhances the level of feedback signal **W** with respect to input signal **X** and hence the noise generating effect of feedback signal **W** on input signal **X**.

As will be appreciated from the foregoing, the quantization circuit 2000 of the present invention provides for a greatly simplified implementation particularly with respect to ASIC implementation. The elimination of the pseudorandom noise generator previously required for dithering techniques and advantageous selection of filter design minimize required gates in the ASIC.

A wideband frequency signal digitizer and method for digitizing a wideband frequency signal provide for optimally positioning a segment of the wideband frequency signal within a Nyquist band of an analog-to-digital converter. Remaining segments of the wideband frequency signal are closely positioned relative to the first segment such that the entire wideband frequency signal is easily digitized using a single or multiple analog-to-digital converters operating at reduced sampling rates while concomitantly reducing or eliminating undesirable spurious signals from the resulting digitized signal.

The following detailed description is presented with reference to digitizer and method for efficiently and accurately digitizing the split portions of the cellular communication system A-band frequency band. It will readily appreciated by one of ordinary skill in the art, however, that the present invention has application to digitizing any wideband signal occupying continuous or discontinuous spectrum. Moreover, while the present invention is described as operating on two segments of the wideband signal, the present invention is equally

applicable to a wideband frequency signal separated into a plurality of segments and processed via a plurality of signal paths.

Referring to Fig. 24, a wideband frequency signal digitizer 2410 in accordance with a preferred embodiment of the present invention is shown. An analog signal is received at antenna 2412 and is signal conditioned through filters 2414 and 2418 and amplifier 2416 as is known in the art. The conditioned analog signal is communicated to mixer 2420 where it is mixed with a signal from local oscillator 2422. This converts, or frequency translates, the received and conditioned signal to an intermediate frequency (IF) signal.

The translated (IF) signal is then communicated to splitter 2424 where the translated signal is split into a first segment and a second segment. The second segment is filtered through filter 2426 and mixed with a second local oscillator 2428 signal in mixer 2430. The second segment is then filtered in filter 2431 and communicated to summer 2434. The first segment signal is filtered through filter 2432 and is also communicated to summer 2434. The first and second segments are summed and then digitized through analog-to-digital converter 2436 at a sampling frequency f_S.

The operation of mixers 2420 and 2430 is to frequency translate the segments of the wideband frequency signal such that it can be digitized This is illustrated in and the operation of digitizer 2410 described with reference to FIGs. 27A and 27B. The spectrum 2700 illustrated in FIG. 27A is typical of the signal received at antenna 2412 for the cellular A-band after processing through filters 2414 and 2418 and amplifier 2416. The spectrum 2700' illustrated in FIG. 27B represents the spectrum of FIG. 27A after processing through mixers 2420 and 2430. The spectrum 2700' is translated to an IF frequency which is within a Nyquist band of the analog-to-digital converter. The wider portion, 2702 of the spectrum 2700' is positioned closely adjacent the sampling frequency f_S. The narrow portion 2704 of spectrum 2700' is split from spectrum 2700' and processed as a separate segment. The result of mixer 2430 is to translate the second

segment 2704 of the wideband frequency signal to a position nearly adjacent the first segment 2702, as can be seen. The first and second segments 2702 and 2704 so positioned may then be digitized with a single ADC at a sampling rate slightly greater than the total bandwidth of the first and second segments. That is the minimum sampling rate:

$$f_S = 2 * (BW_W + BW_n) \text{ MHz} \qquad \text{(a)}$$

where BWw, BWn are as shown and where a separation band BW_g 406 is provided between the first and second segments 2702 and 2704 for filtering. The first and second segments may only be placed as closely adjacent as is possible without portions of the first and second segments falling within the transition regions of the filters.

The transition region of the analog filter is illustrated in FIG. 27A. The transition region begins at the edge of the band segment and extends to a point, "A". Point "A" represents an attenuation point which, in the preferred embodiment, is approximately 80 decibels (dB), which is defined as the "alias point", i.e., the point at which signals at frequencies falling outside of the filtered region would produce undesirable aliases in the digitized spectrum.

With reference now to FIG. 25, a second embodiment of a wideband frequency digitizer 2500 according to the present invention is shown. Signals are received at antenna 2512 and are processed through filter 2514 and amplifier 2516. The signal is split in splitter 2518 into first and second segments which are communicated to first and second signal paths 2520 and 2522, respectively. The first segment is filtered through filter 2524 and is mixed with a local oscillator 2528 signal in mixer 2526. The mixed first segment signal is then filtered through filter 2530 and is digitized in ADC 2532 at a first sampling rate, f_S. The digitized first segment is then filtered through digital filter 2534 and is communicated to summer 2550.

The second segment of the signal, communicated along signal path 2522, is filtered through filter 2536 and mixed with a local oscillator 2540 signal in mixer 2538. The signal is then filtered again through filter 2542 and digitized in ADC 2544 at a sampling rate of

$f_S/2$. The resulting digital signal is then digitally filtered through digital filter 2546 and interpolated to f_S and high pass filtered in interpolator/filter 2548. The resulting signal is then communicated to summer 2550 where it is summed with the digitized first segment of the signal yielding the entire digitized signal.

Digitizer 2500 is preferable were the second segment of the signal has bandwidth smaller than the transition region and less than half the bandwidth of the first segment. This is illustrated and the operation of 2500 will be described with reference to FIGs. 28A-28H. The left and right sides of FIGs. 28A-28H illustrate separately the processing of a received signal by digitizer 2500 as occurs along signal paths.

FIGs. 28A and 28D illustrate separate segments 2802 and 2804 of a received signal. With reference to FIG. 28A, segment 2802 is the result of processing the signal along first signal path 2520 through filter 2530. Segment 2802 is then digitized by ADC 2432 at a sampling rate f_S resulting in the digital signal portions 2806 illustrated in FIG. 28B. Sampling rate f_S is chosen as approximately 2.5 times the bandwidth of segment 2802. These signal portions are then digital filtered through filter 2534 as shown in FIG. 28C to remove any undesirable frequency components from the digital signals.

Segment 2804 is the result of processing the signal along the second signal path 2522 through filter 2542. Segment 2804 is then digitize through ADC 2446 at a sampling rate of $f_S/2$ resulting in the digital signal portions 2808 illustrated in FIG. 28E. The digital signal portions 2808 are first digitally filtered through digital filter 2546 to remove undesirable signal components. Next, the digital signal portions 2808 are interpolated up to a rate of f_S and digitally filtered in interpolator/filter 2548 as illustrated in FIG. 28F to produce a digital signal portion 2810 shown in FIG. 28G. Digital signal portion 2810 is summed with digital signal portions 2806 in summer 2550 resulting in the digital signal spectrum shown in FIG. 28H.

The present invention advantageously combines analog filtering prior to digitizing and followed by digital filtering of split segments of a signal to be digitized. Digital filtering offers the advantage of allowing the digitized signal portions to be positioned closely adjacent spectrally for reducing sampling frequency and data rates.

With reference now to FIG. 26, a third embodiment of a wideband frequency digitizer 2600 according to the present invention is shown. Digitizer 2600 includes two signal paths 2620 and 2622 which are generally equivalent to those of digitizer 2500 with the processing of the signal after the ADC being modified. Signals are received at antenna 2612 and are processed through filter 2614 and amplifier 2616. The signal is split in splitter 2618 into first and second segments which are communicated to the first and second signal paths 2620 and 2622, respectively. The first segment is filtered through filter 2624 and is mixed with a local oscillator 2628 signal in mixer 2626. The mixed first segment signal is then filtered through filter 2630 and is digitized in ADC 2632 at a first sampling rate, f_S. The digitized first segment is then filtered through digital filter 2634, interpolated by 3 in interpolator 2636, low pass filtered through digital filter 2638 and decimated to 1.5 f_S in decimator 2640 then communicated to summer 2650.

The second segment of the signal, communicated along signal path 2622, is filtered through filter 2642 and mixed with a local oscillator 2646 signal in mixer 2644. The signal is then filtered again through filter 2648 and digitized in ADC 2652 at a sampling rate of $f_S/2$. The resulting digital signal is then low pass filtered through digital filter 2654 and interpolated to 1.5 f_S in interpolator 2656 and high pass filtered in filter 2660. The resulting signal is then communicated to summer 2650 where it is summed with the digitized first segment of the signal yielding the entire digitized signal at 1.5 f_S.

Digitizer 2600 is preferred where the second, smaller band segment is greater than the transition region but less than the half the bandwidth of the first segment. Where the second, smaller band

segment is greater than the half the first band segment, digitizer 2600 is modified slightly. The second signal is digitized at the sampling frequency f_S. As will be further appreciated, the interpolators 2636 and 2656 and decimator 2640 are not required.

Digitizing the second segment under Nyquist criteria would suggest a sampling rate approximately 2 - 2.5 times the bandwidth of the second segment. However, in the present invention, the sampling rate is advantageously chosen as $f_S/2$ which is easily generated from f_S and will not introduce harmonics into band. This sampling rate is chosen even where $f_S/2$ or f_S is higher than is required by Nyquist criteria for the second segment. Local oscillator frequency selection is straight forward, and the frequencies are chosen such that the bands are positioned closely adjacent, spectrally, without overlap as shown in FIGs 4A-4B and 5A-5H. Providing digital filtering simplifies isolating the band segments allowing the segments to be placed very close together.

The preferred embodiments of the present invention were presented with reference to digitizing a frequency band having two segments. It should be understood, however, that a wideband frequency where the wideband frequency can be divided into a number of segments, can be digitized in accordance with the present invention. For example, digitizer 10 is applicable where the segments can be mixed closely adjacent each other in a single Nyquist band. Digitizers 2500 or 2600 are applicable where the segments can not be mixed to within a single Nyquist band by combining a number of signal paths equal to the number of segments to digitize.

Digitizing of a split frequency band analog signal is accomplished in the present invention with both reduced sampling frequency and hardware requirements. The present invention provides for mixing the entire split frequency bandwidth about a reference frequency

which will allow for digitizing at a reduced sampling frequency. The reference frequency is chosen such that the segments of the split frequency bandwidth occupy adjacent aliasing bands. Digitizing at a reduced sampling frequency produces a digital signal with the entire split frequency band signal represented in a single Nyquist band of the sampling frequency.

Referring to FIG. 29 a digital radio receiver 2910 incorporating the digitizer of the present invention is shown. A split frequency band analog signal is received at antenna 2912 and down mixed and signal conditioned through filter 2914 and amplifier 2916 as is well known in the art. The split frequency band signal is then communicated to mixer 2918 where it is frequency translated by a signal from local oscillator 2920.

With reference to FIGs. 30A - 30C, a split frequency band signal 3000 is shown. Signal 3000 is typical of that of the cellular A-band, however, it should be understood that the present invention is applicable to digitizing any type split frequency band analog signal. The result of mixing signal 3000 with the reference frequency in mixer 2918 is signal 3000', FIG. 30B. As can be seen, after mixing, the split frequency band signal is translated such that the split segments of the signal 3000' lie about the reference frequency shown as $f_S/2$. It will be appreciated that an appropriate local oscillator frequency can be selected for either high side or low side injection, depending upon the split band frequency signal, to translate the signal about the reference signal.

The mixed split frequency band signal is further conditioned through filter 2922 and amplifier 2924. The translated split band frequency signal is then communicated to analog-to-digital converter (ADC) 2926. Analog-to-digital converter 2926, digitizes at a sampling rate f_S, in a known manner, the split frequency band analog signal to produce a digital signal 2927. Digital signal 2927 is represented in FIG. 30C as 3000". As can be seen from FIG. 30C, digitizing signal 3000' results in aliasing of the split band segments

(shown in phantom) of signal 3000', with the aliased segments contained within a Nyquist band of the sampling frequency, fs.

In the preferred embodiment of the present invention, the sampling frequency, fs, is selected to be approximately 2.5 times the bandwidth of the wider segment of the split band frequency signal. The reference frequency is selected to be approximately half the sampling frequency or a multiple thereof. As will be appreciated, the entire split frequency band signal is digitized using a sampling rate which is less than twice the total spectral bandwidth of the split frequency band signal, e.g., as shown in FIG. 30A. With further reference to FIG. 30C a specific example of selecting the sampling frequency is shown for the cellular A-band. From the spectral chart shown, two observations can be made, first:

$$X + 1.5 + 2Y = 10 \qquad (a)$$

and second:

$$Z + 11 + X + 1.5 + Y = f s/2 \qquad (b)$$

from which it can be determined that:

$$f s = 33.5 + X + 2Z \qquad (c)$$

where X, Y and Z are as shown in FIG. 30C, and 11 MHz and 1.5 MHz are the bandwidths of the segments being digitized, respectively. This relationship is true regardless of the alias band being considered.

It can be seen from the above that fs can approach 33.5 Ms/s as compared to 56 Ms/s which would otherwise be required to digitized the cellular A-band. In practical applications, fs is dependent on filtering. That is, the X segment must be wide enough to allow an anti-aliasing filter to pass the 11 MHz band but attenuate the 1.5 MHz alias. The Z segment must be big enough such that, after mixing, the image that is generated by sampling can be filtered out. In practice, fs can realistically approach 35 Ms/s.

The digital signal 3000" is then communicated to channel processors 2928. Channel processors operate on signal 3000" to recover the digital representation of the entire split frequency band

signal. A discussion of such channel processors can be found in the afore-mentioned U.S. Patent Application entitled "Multi-channel Digital Transceiver and Method". It should be noted that the digital representation of the signal, due to aliasing contains transposed segments of the split frequency band signal. It would, however, be within the skilled artisans knowledge to properly reconstruct the split frequency band signal from these transposed segments.

With reference then to FIG. 31, a method of digitizing a split frequency band signal in accordance with a preferred embodiment of the present invention is shown, 3100-3108. A split frequency band signal is received, 3102, and is mixed 3104 such that the translated split frequency band signal segments lie about a reference frequency. The mixed signal is then digitized, 3106, producing a digital signal including aliases of the split frequency band signal. The mixed signal is digitized a sampling rate which is less than twice the total bandwidth of the split frequency band signal. The split frequency band signal is then recovered from the digital signal in a channel processor card 3108.

The many advantages and features of the present invention will be appreciated from the foregoing description of several preferred embodiments. It should be understood, that many other embodiments, advantages and features fall within its fair scope as may be understood from the subjoined claims.

What is claimed is:

CLAIMS

1. A digital receiver comprising:

a plurality of antennas for receiving radio frequency signals;

a plurality of analog to digital converters responsive to the plurality of antennas;

a switched digital downconverter responsive to the plurality of analog to digital converters; and

a channel processor responsive to the switched digital downconverter.

2. The digital receiver of claim 1, further comprising a first mixer coupled to receive an analog split frequency band signal, the split frequency signal having a first segment having a first bandwidth and a first center frequency, a second segment having a second bandwidth and a center frequency, and a total bandwidth greater then the sum of the first and second bandwidths, the mixer mixing the received signal with a reference frequency to produce a frequency translated signal, the reference frequency located between the first center frequency and the second center frequency; and

wherein the analog-to-digital converter is responsive to the mixer, the analog-to-digital converter digitzing the frequency translated signal by sampling the frequency translated signal at a sampling rate less than twice the total bandwidth of the split frequency band signal to produce a digital signal, the digital signal including the first and second segments and aliased versions of the first and second segments of the split frquency band signal.

3. The digital receiver of claim 2, wherein the first and second segments and the aliased versions of the first and second segments are all spectrally located within a bandwidth that is less than the total bandwidth of the analog split frequency band signal wherein the reference frequency is a multiple of the Nyquist frequency.

4. A digital transmitter comprising:

a channel processor;

a plurality of upconverters responsive to the channel processor;

a plurality of digital to analog converters responsive to the plurality of upconverters; and

a plurality of antennas responsive to the plurality of digital to analog converters.

5. The digital transmitter of claim 4, further comprising a plurality of digital summers responsive to the plurality of upconverters.

6. The digital transmitter of claim 4, further comprising an analog summer responsive to the plurality of digital to analog converters.

7. The digital transmitter of claim 6, further comprising a radio frequency upconverter responsive to the analog summer.

8. The digital transmitter of claim 7, further comprising a plurality of power amplifiers responsive to the radio frequency upconverter and coupled to at least one of the plurality of antennas.

9. A digital transmitter comprising:

an upconverter/modulator comprising:

a first selector and a second selector;

a first interpolation filter responsive to the first selector and a second interpolation filter responsive to the second selector;

a first mixer responsive to the first interpolation filter;

a second mixer responsive to the second interpolation filter; and

an output adder responsive to the first and second mixer; and

a digital switch responsive to the upconverter/modulator.

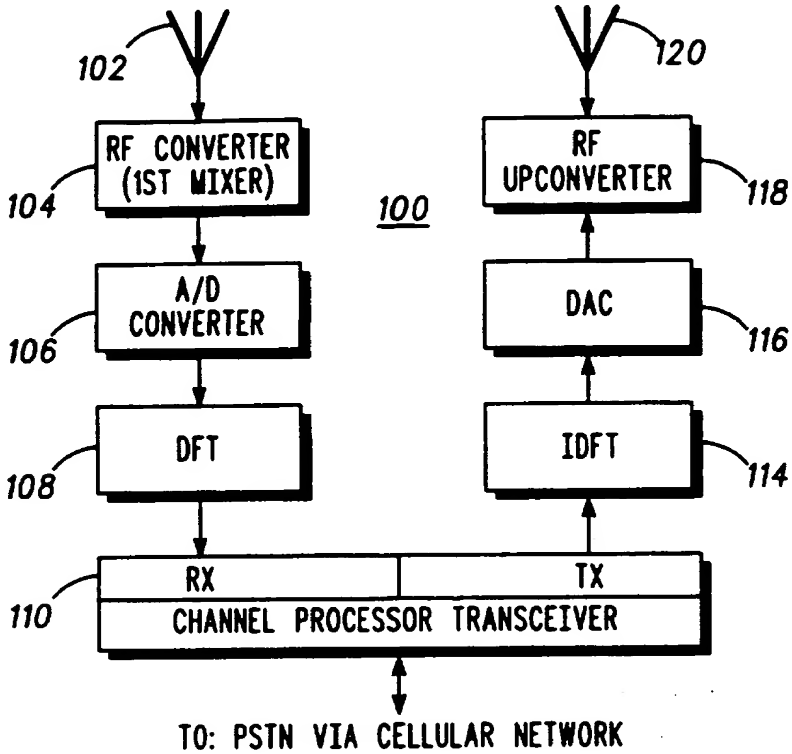


FIG.1
—PRIOR ART—

FIG.2

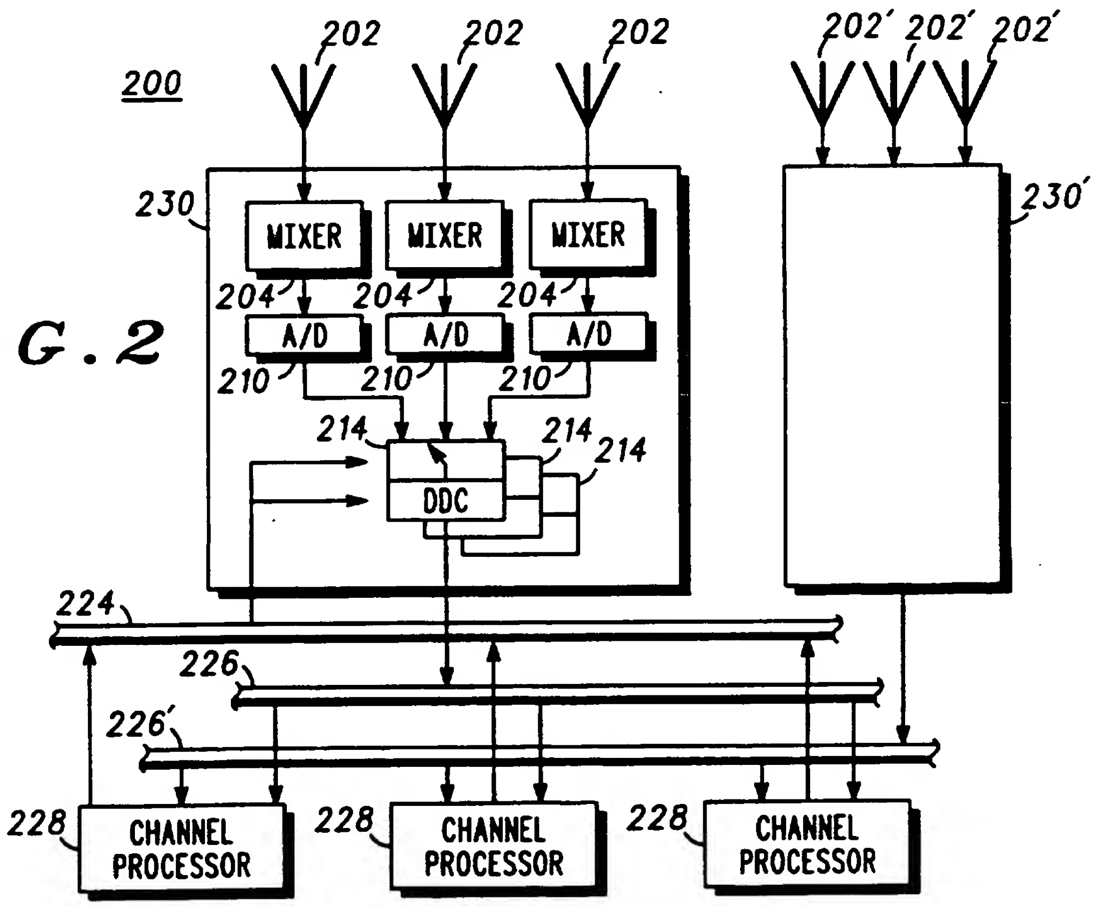


FIG.3

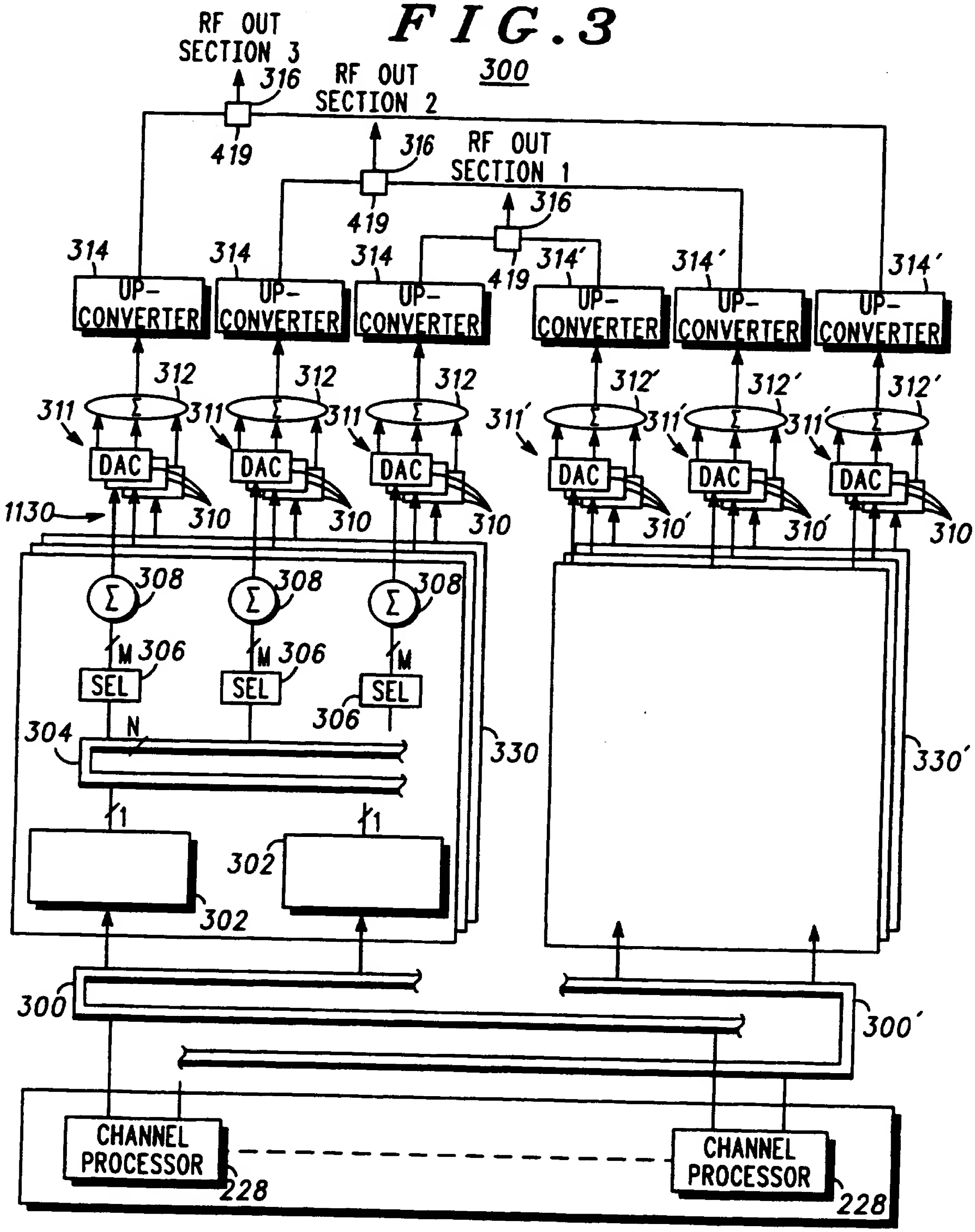
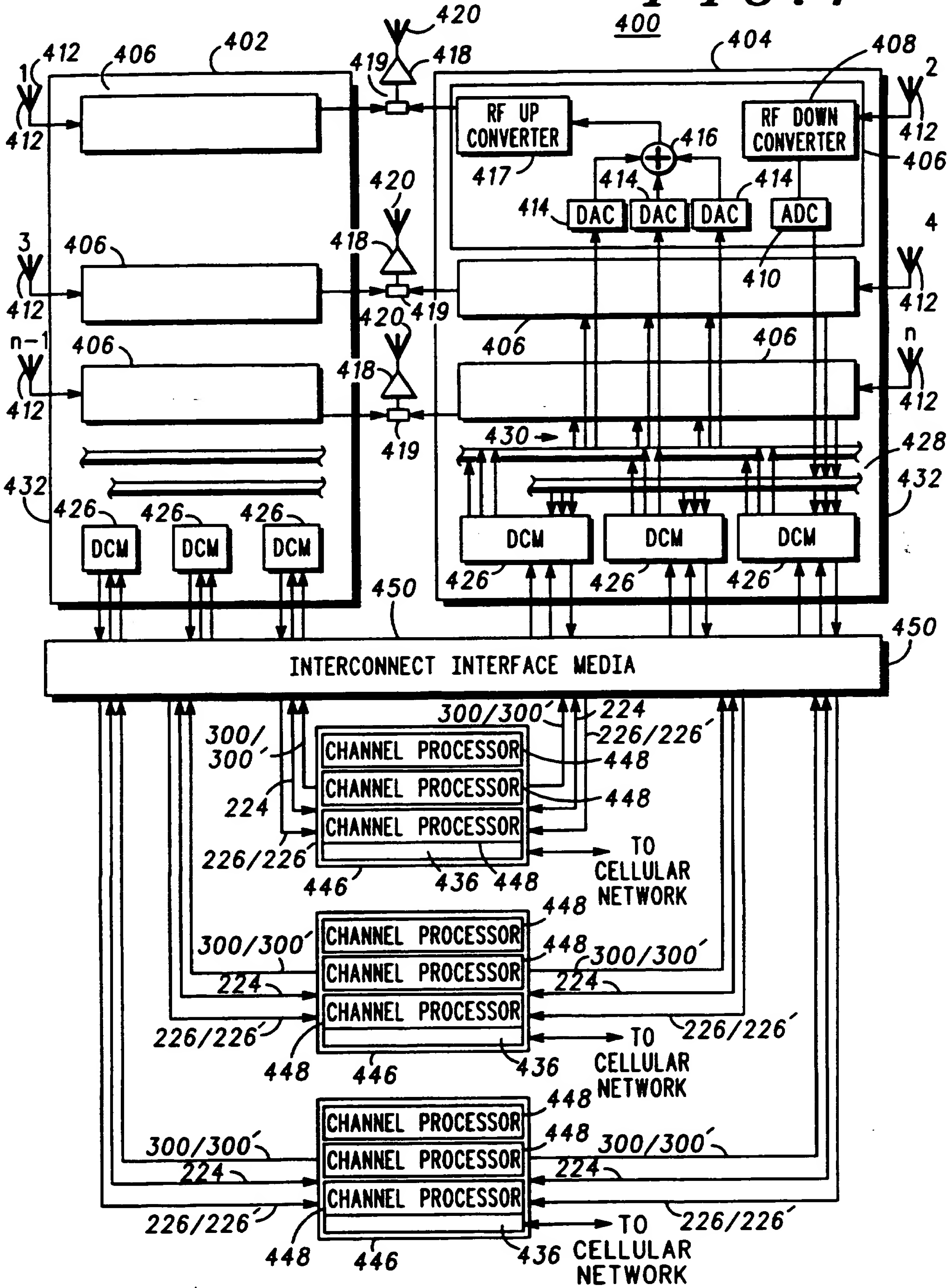

RF OUT SECTION 3
316
RF OUT SECTION 2
300
419
316
RF OUT SECTION 1
419
316
314
314
314
419
314'
314'
314'
UP-CONVERTER
UP-CONVERTER
UP-CONVERTER
UP-CONVERTER
UP-CONVERTER
UP-CONVERTER
312
312
312
312'
312'
312'
311
311
311
311'
311'
311'
Σ
DAC
DAC
DAC
DAC
DAC
DAC
1130
310
310
310
310'
310'
310'
308
308
308
Σ
M 306
M 306
M
SEL
SEL
SEL
306
304
N
330
330'
1
1
302
302
300
300'
CHANNEL PROCESSOR
228
CHANNEL PROCESSOR
228

FIG.4


400
402
404
406
408
RF UP CONVERTER
RF DOWN CONVERTER
416
417
414
DAC
DAC
DAC
ADC
410
412
418
419
420
1
2
3
4
n-1
n
430
428
432
426
DCM
DCM
DCM
DCM
DCM
DCM
450
INTERCONNECT INTERFACE MEDIA
300/300'
224
226/226'
CHANNEL PROCESSOR
CHANNEL PROCESSOR
CHANNEL PROCESSOR
448
446
436
TO CELLULAR NETWORK
CHANNEL PROCESSOR
CHANNEL PROCESSOR
CHANNEL PROCESSOR
TO CELLULAR NETWORK
CHANNEL PROCESSOR
CHANNEL PROCESSOR
CHANNEL PROCESSOR
TO CELLULAR NETWORK

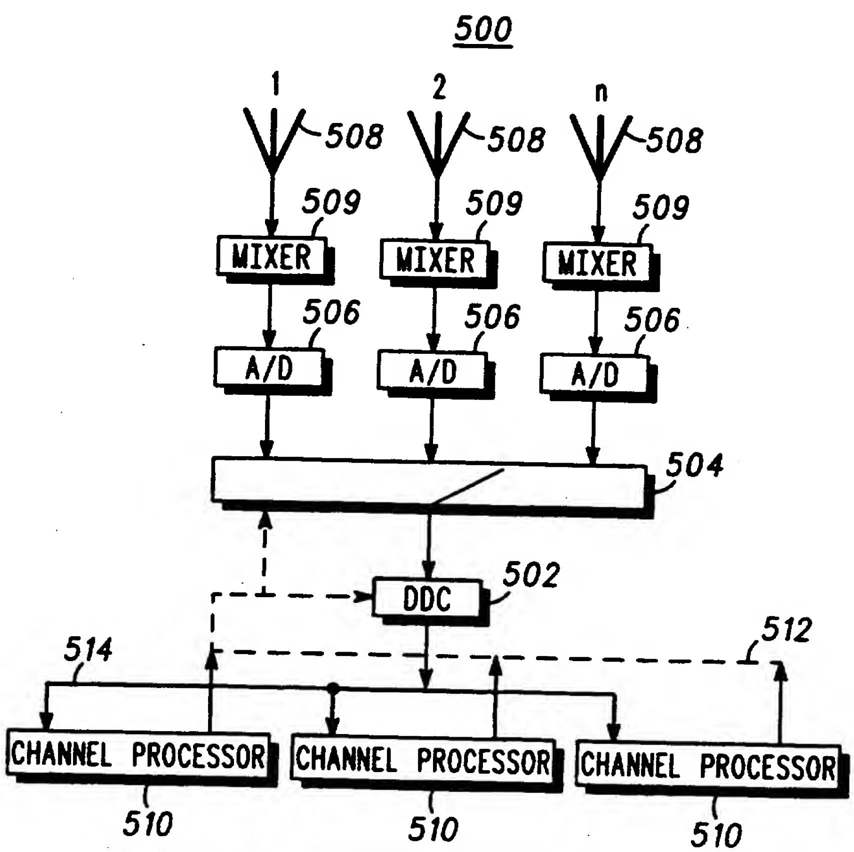
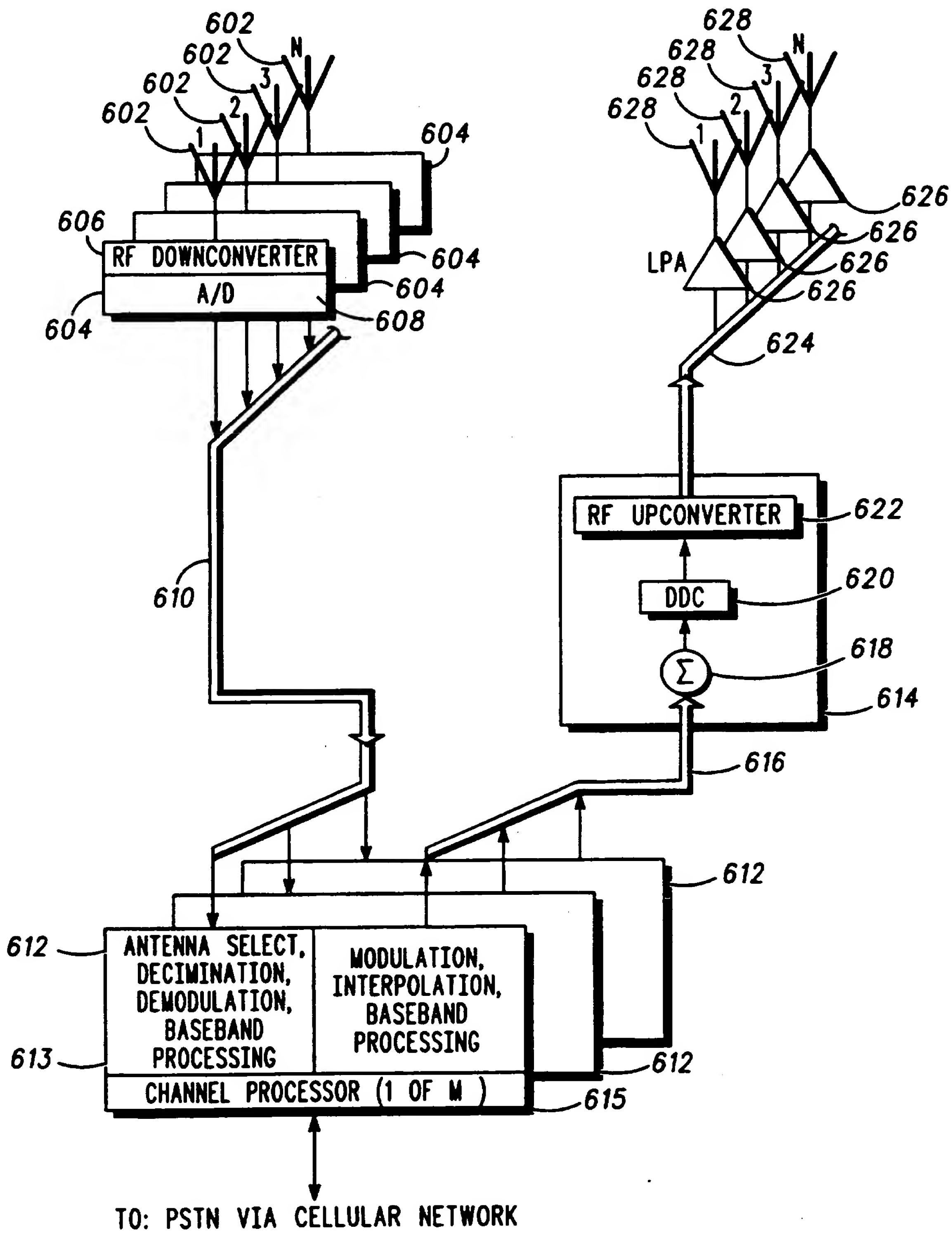

500
1
2
n
508
508
508
509
509
509
MIXER
MIXER
MIXER
506
506
506
A/D
A/D
A/D
504
DDC
502
512
514
CHANNEL PROCESSOR
CHANNEL PROCESSOR
CHANNEL PROCESSOR
510
510
510

FIG. 5

FIG.6


602
602
602
602
1
2
3
N
604
604
604
604
606
RF DOWNCONVERTER
A/D
608
610
628
628
628
628
1
2
3
N
626
626
626
626
LPA
624
RF UPCONVERTER
622
DDC
620
Σ
618
614
616
612
612
612
613
ANTENNA SELECT, DECIMINATION, DEMODULATION, BASEBAND PROCESSING
MODULATION, INTERPOLATION, BASEBAND PROCESSING
CHANNEL PROCESSOR (1 OF M)
615
TO: PSTN VIA CELLULAR NETWORK

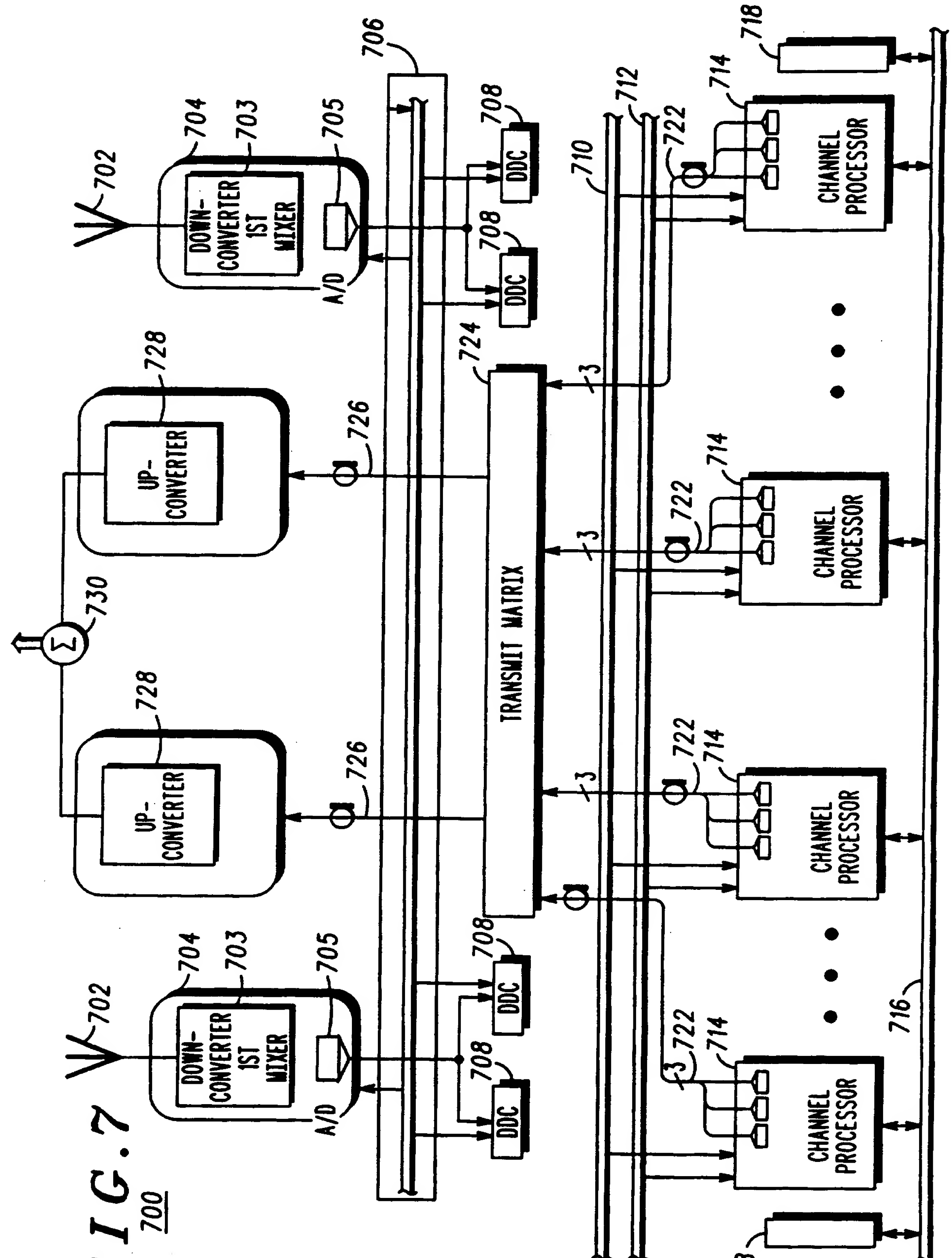

702
704
703
705
DOWN-CONVERTER 1ST MIXER
A/D
706
708
DDC
DDC
728
UP-CONVERTER
UP-CONVERTER
726
730
Σ
724
TRANSMIT MATRIX
3
710
712
722
714
CHANNEL PROCESSOR
CHANNEL PROCESSOR
CHANNEL PROCESSOR
CHANNEL PROCESSOR
716
718

FIG. 7
700

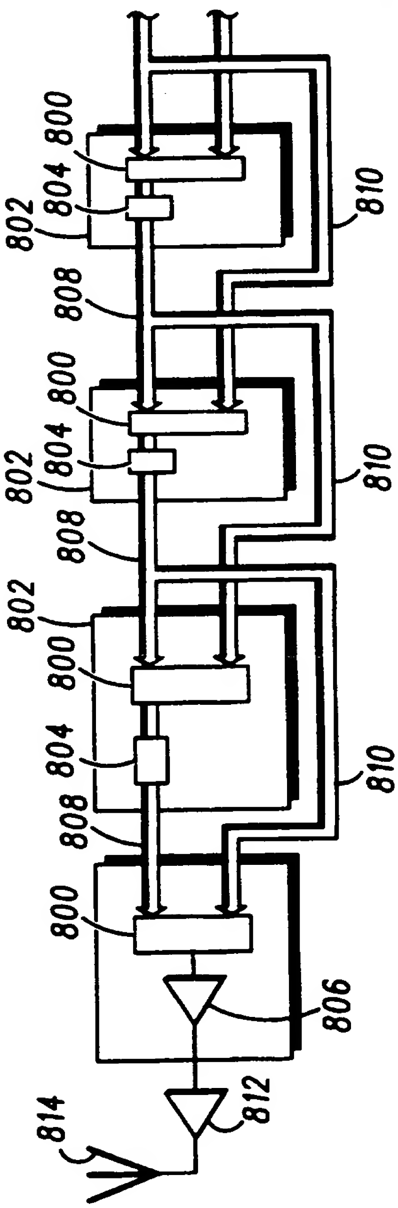


FIG. 8

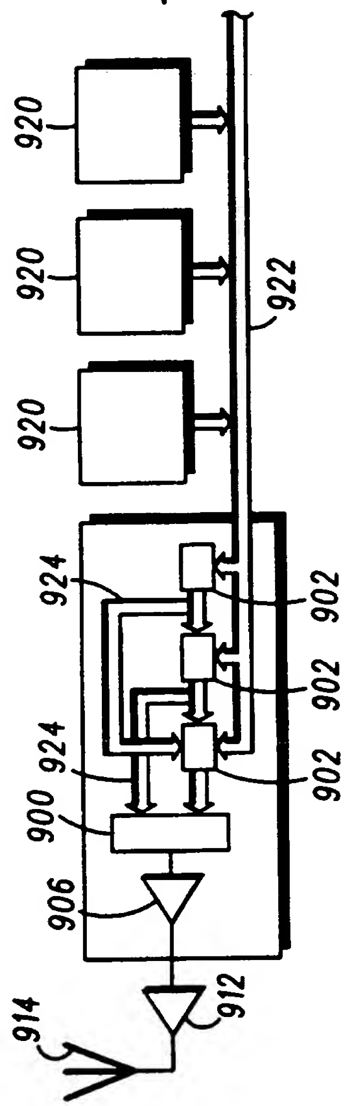


FIG. 9

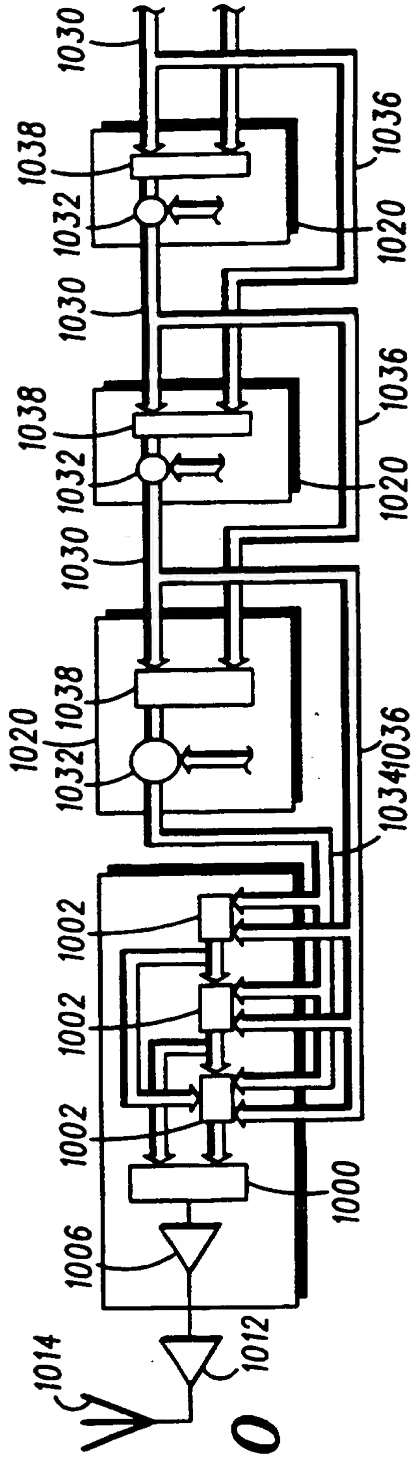


FIG. 10

FIG. 11

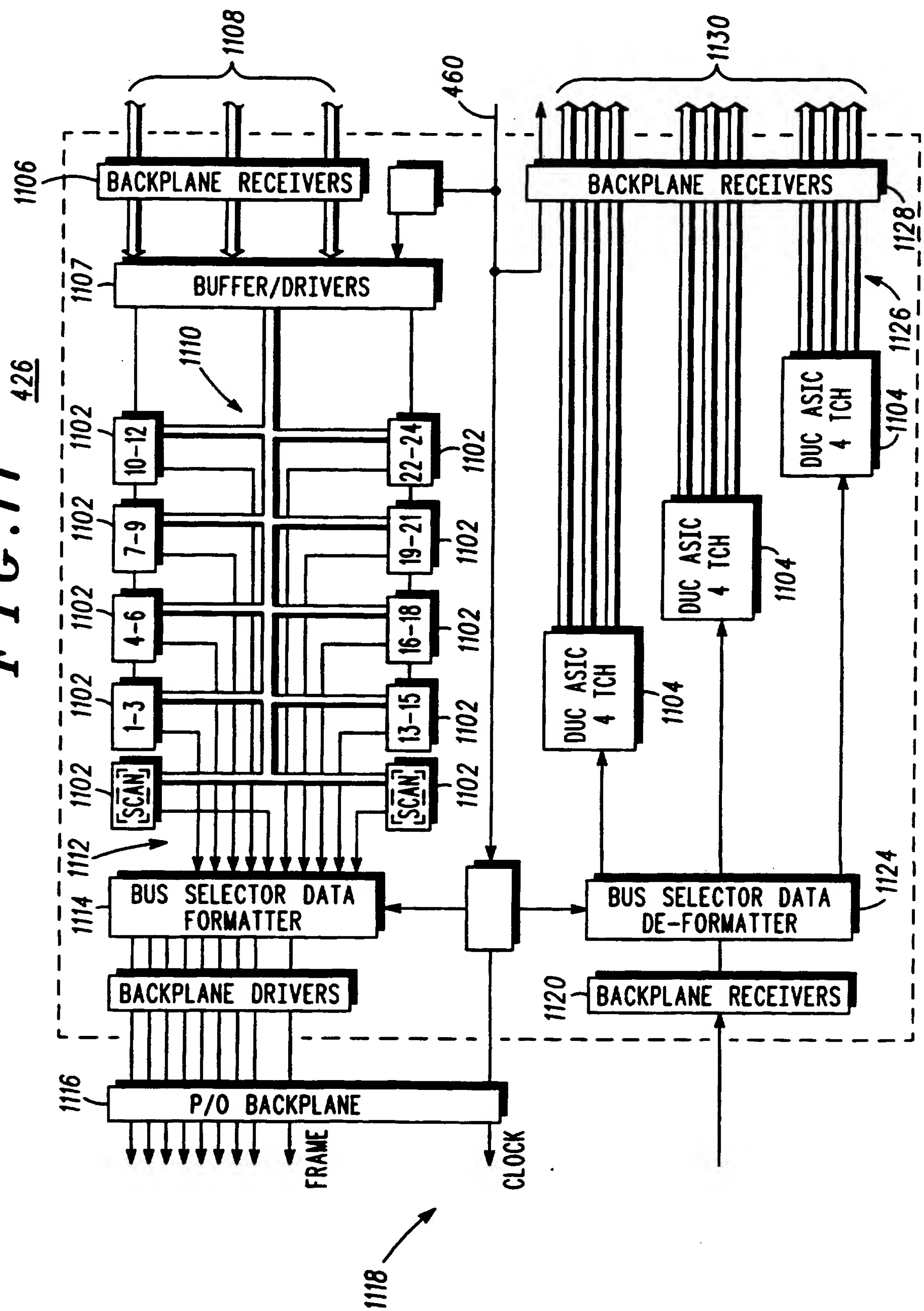
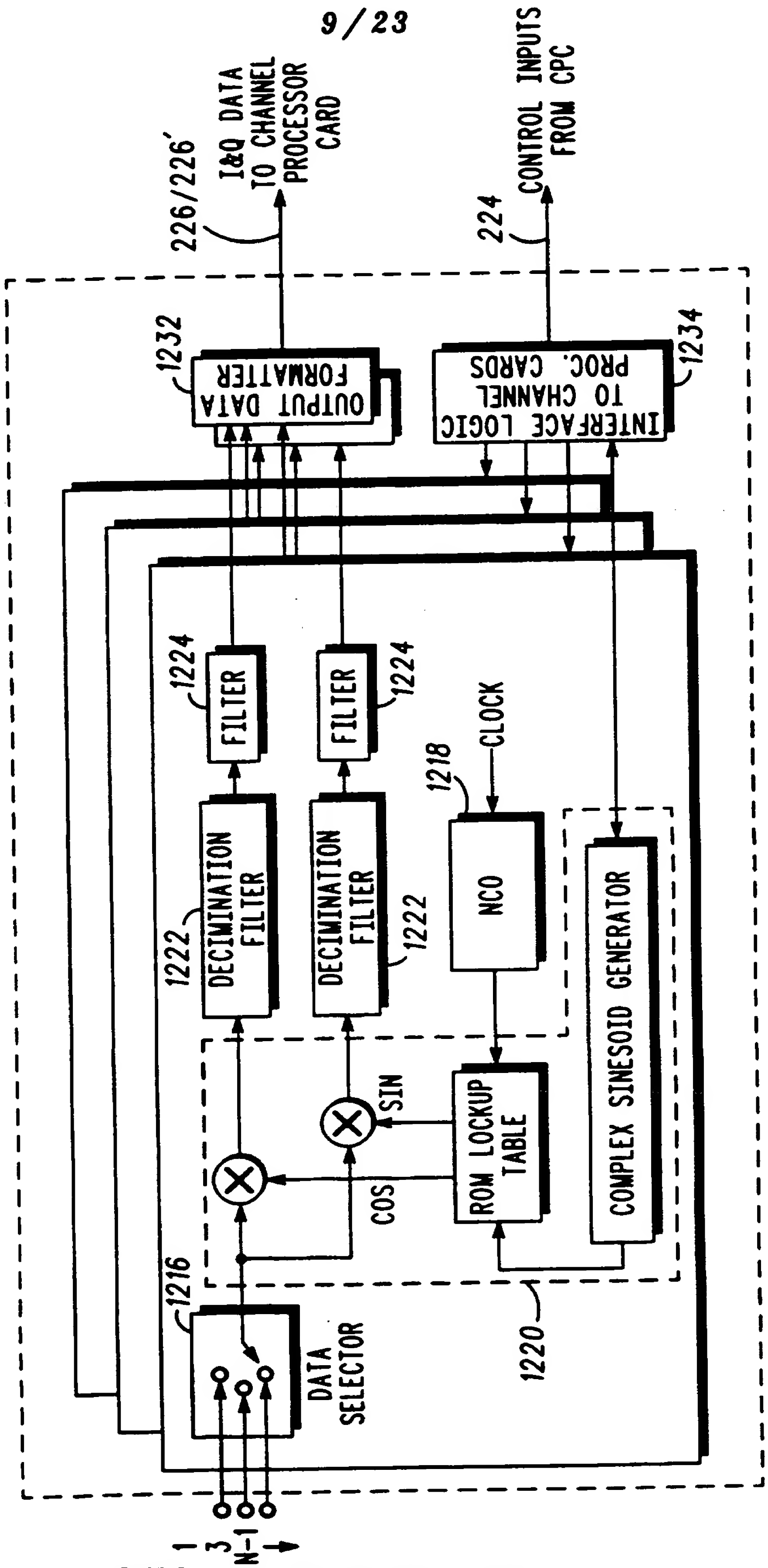

426
1108
1130
460
1106
BACKPLANE RECEIVERS
BACKPLANE RECEIVERS
1128
1107
BUFFER/DRIVERS
1110
1126
1102
10-12
7-9
4-6
1-3
SCAN
22-24
19-21
16-18
13-15
SCAN
DUC ASIC 4 TCH
1104
1112
1114
BUS SELECTOR DATA FORMATTER
BUS SELECTOR DATA DE-FORMATTER
1124
BACKPLANE DRIVERS
1120
BACKPLANE RECEIVERS
1116
P/O BACKPLANE
FRAME
CLOCK
1118

FIG.12



I&Q DATA TO CHANNEL PROCESSOR CARD
226/226'
CONTROL INPUTS FROM CPC
224
OUTPUT DATA FORMATTER
1232
INTERFACE LOGIC TO CHANNEL PROC. CARDS
1234
FILTER
1224
FILTER
1224
DECIMINATION FILTER
1222
DECIMINATION FILTER
1222
CLOCK
1218
NCO
COMPLEX SINESOID GENERATOR
SIN
COS
ROM LOCKUP TABLE
1216
DATA SELECTOR
1220
1
3
N-1

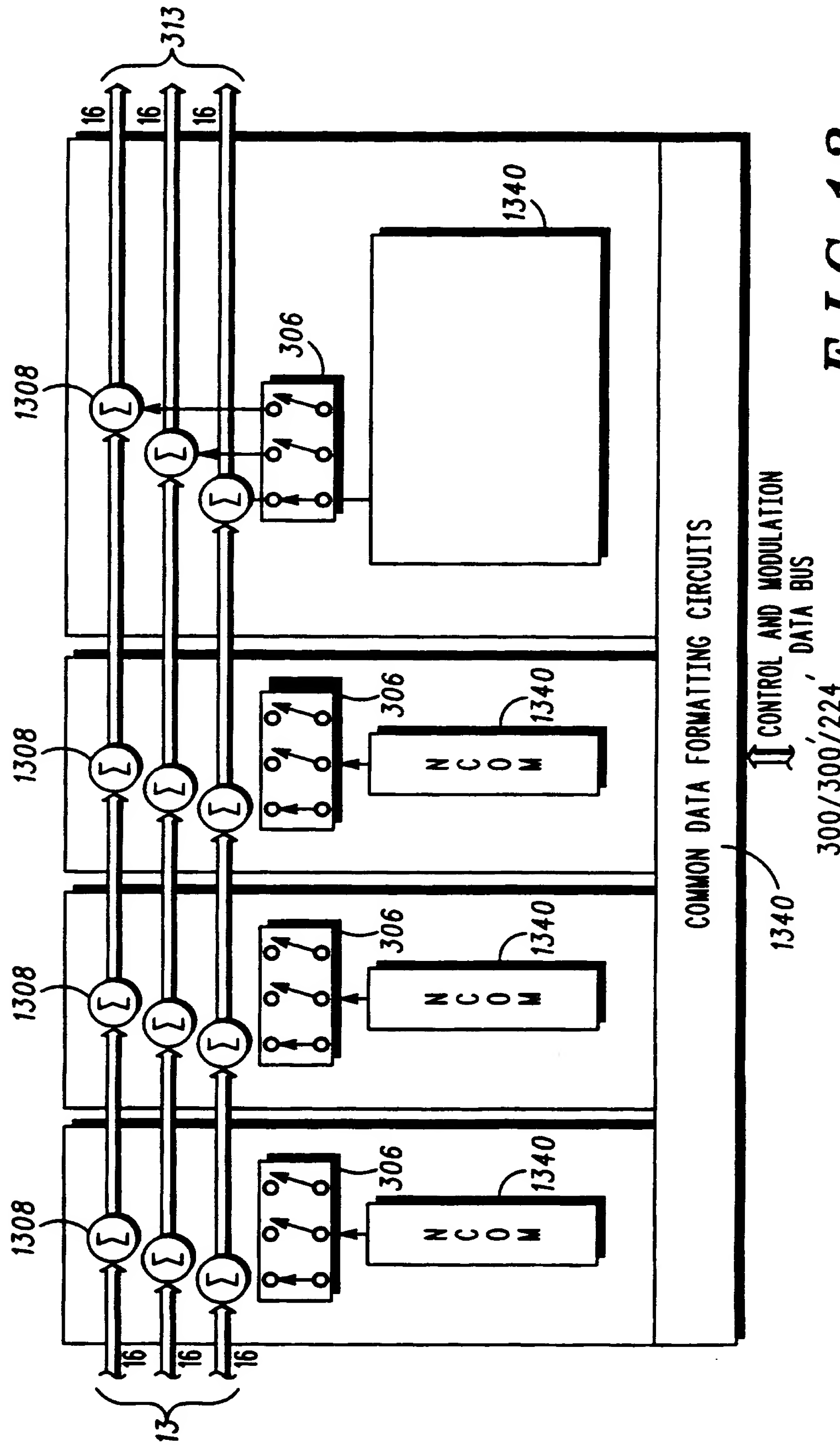

302
313
16
16
16
1308
306
1340
NCOM
COMMON DATA FORMATTING CIRCUITS
CONTROL AND MODULATION DATA BUS
300/300'/224'
313

FIG.13

FIG.14

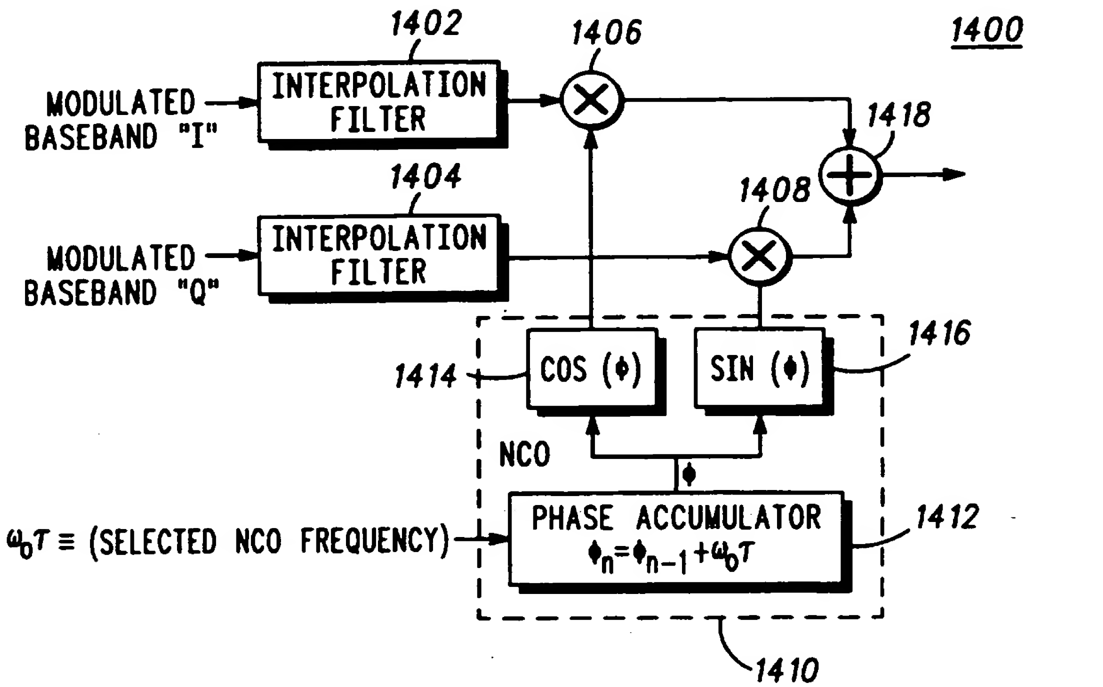
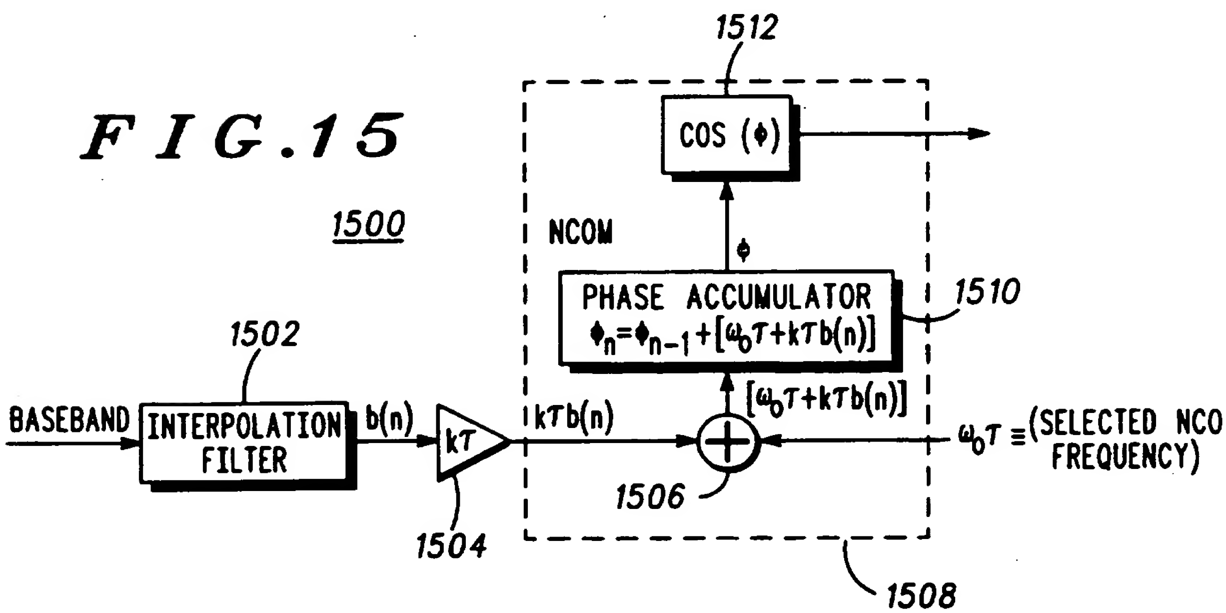
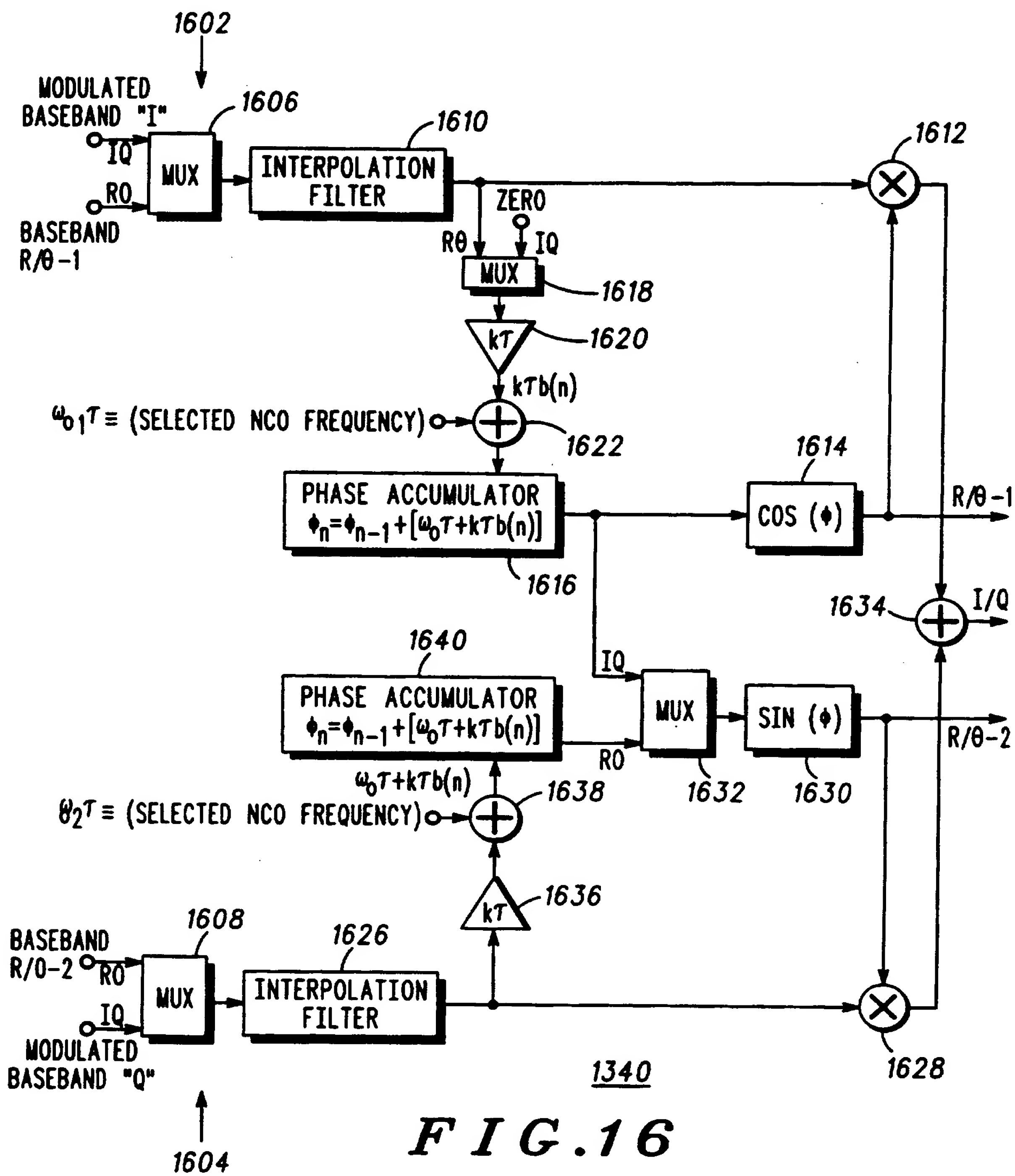

1400
1402
1406
MODULATED BASEBAND "I"
INTERPOLATION FILTER
1418
1404
1408
MODULATED BASEBAND "Q"
INTERPOLATION FILTER
1416
1414
COS (ϕ)
SIN (ϕ)
NCO
ϕ
$\omega_0 T \equiv$ (SELECTED NCO FREQUENCY)
PHASE ACCUMULATOR
$\phi_n=\phi_{n-1}+\omega_0 T$
1412
1410

FIG.15


1500
1512
COS (ϕ)
NCOM
ϕ
PHASE ACCUMULATOR
$\phi_n=\phi_{n-1}+[\omega_0 T+kTb(n)]$
1510
1502
$[\omega_0 T+kTb(n)]$
BASEBAND
INTERPOLATION FILTER
b(n)
kT
kTb(n)
$\omega_0 T \equiv$ (SELECTED NCO FREQUENCY)
1506
1504
1508



1602
MODULATED BASEBAND "I"
1606
IQ
RO
MUX
BASEBAND R/θ-1
INTERPOLATION FILTER
1610
1612
ZERO
Rθ
IQ
MUX
1618
kT
1620
kTb(n)
$\omega_{01}T \equiv$ (SELECTED NCO FREQUENCY)
1622
1614
PHASE ACCUMULATOR
$\phi_n=\phi_{n-1}+[\omega_0T+kTb(n)]$
COS (ϕ)
R/θ-1
1616
1634
I/Q
1640
IQ
PHASE ACCUMULATOR
$\phi_n=\phi_{n-1}+[\omega_0T+kTb(n)]$
MUX
SIN (ϕ)
R/θ-2
RO
$\omega_0T+kTb(n)$
1638
1632
1630
$\theta_2T \equiv$ (SELECTED NCO FREQUENCY)
1636
kT
1608
1626
BASEBAND R/0-2
RO
MUX
IQ
INTERPOLATION FILTER
MODULATED BASEBAND "Q"
1628
1340
1604

FIG.16

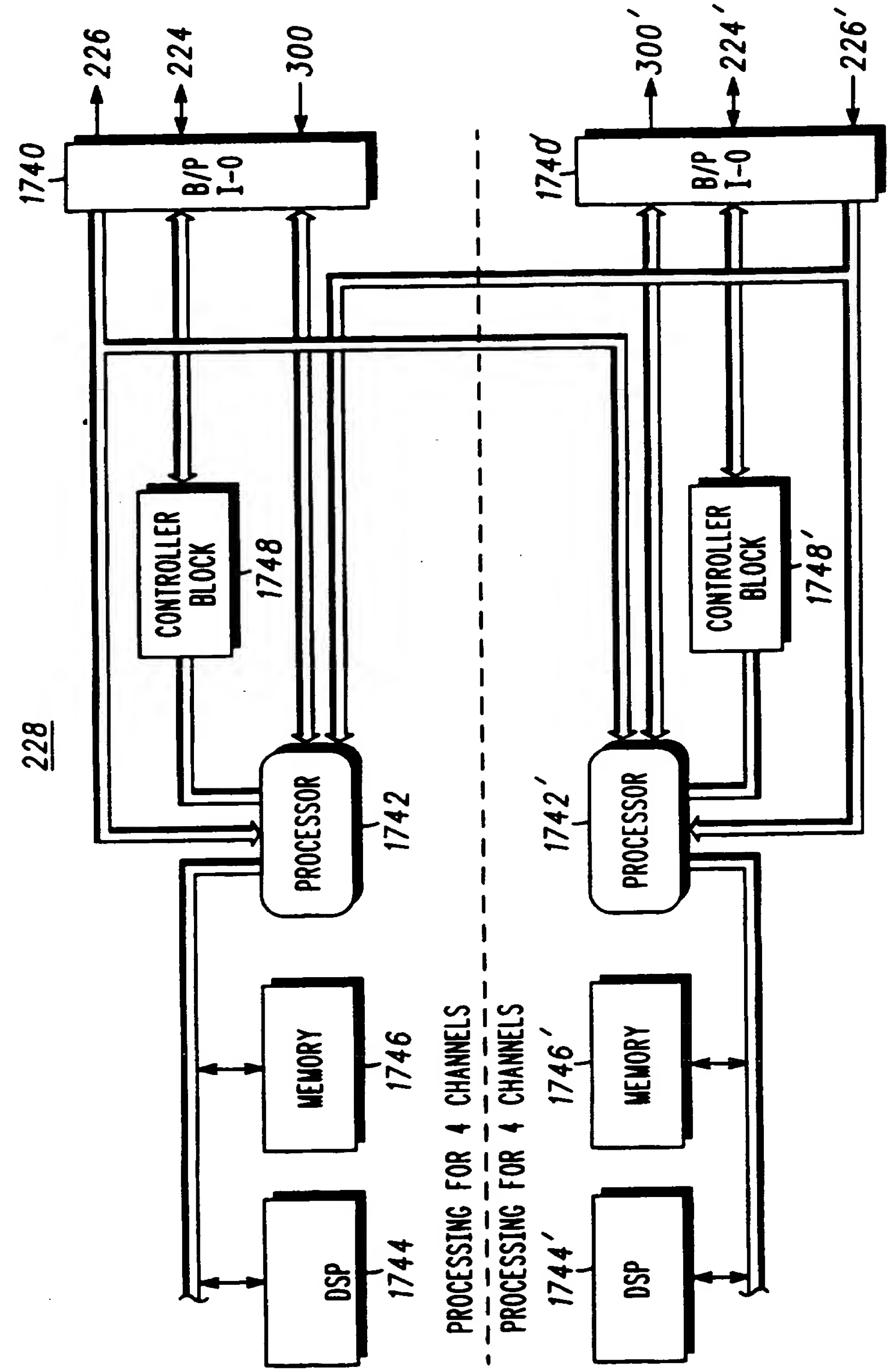

228
1740
B/P I-O
226
224
300
1740'
B/P I-O
300'
224'
226'
CONTROLLER BLOCK
1748
CONTROLLER BLOCK
1748'
PROCESSOR
1742
PROCESSOR
1742'
MEMORY
1746
MEMORY
1746'
DSP
1744
DSP
1744'
PROCESSING FOR 4 CHANNELS
PROCESSING FOR 4 CHANNELS

FIG.17

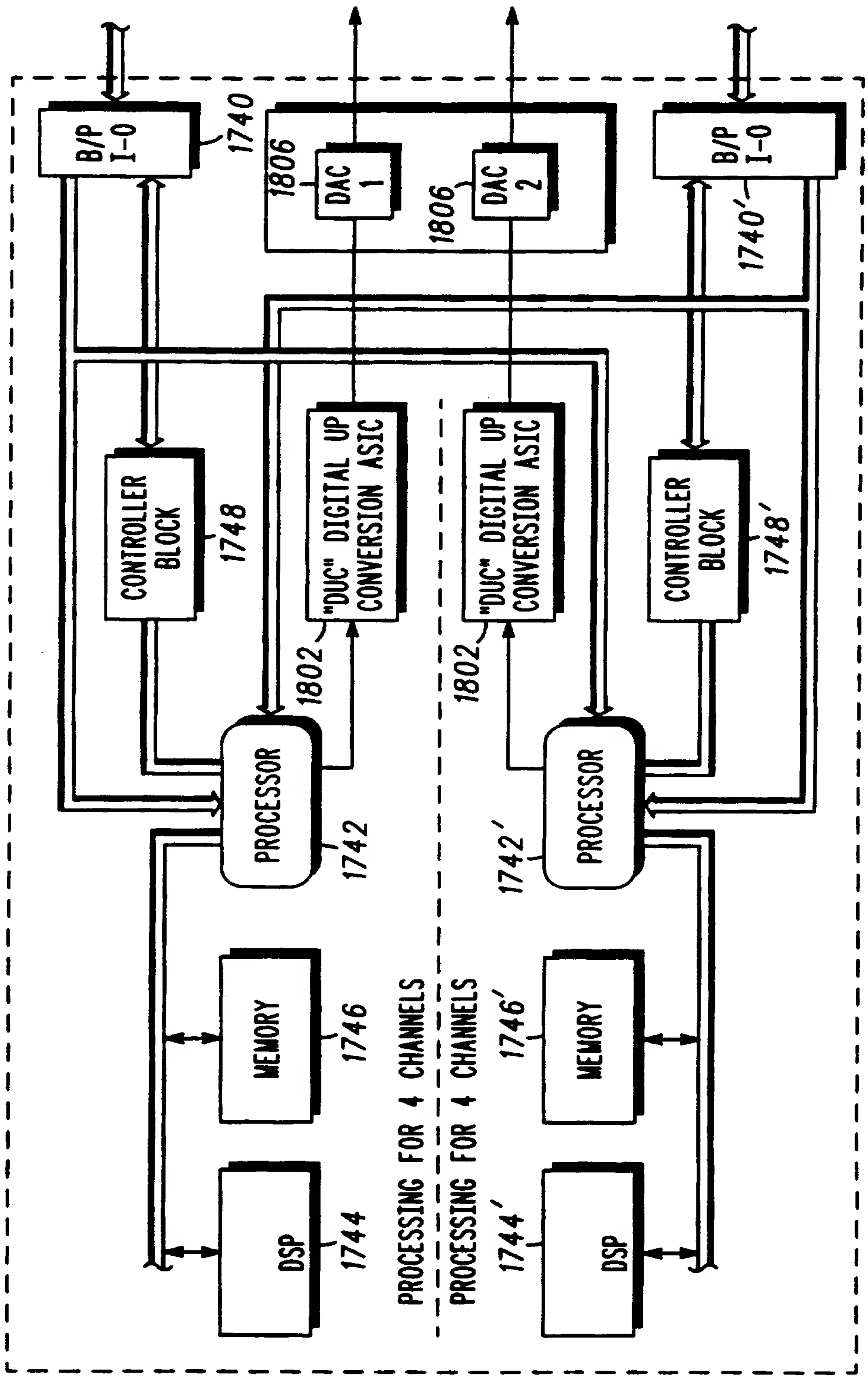
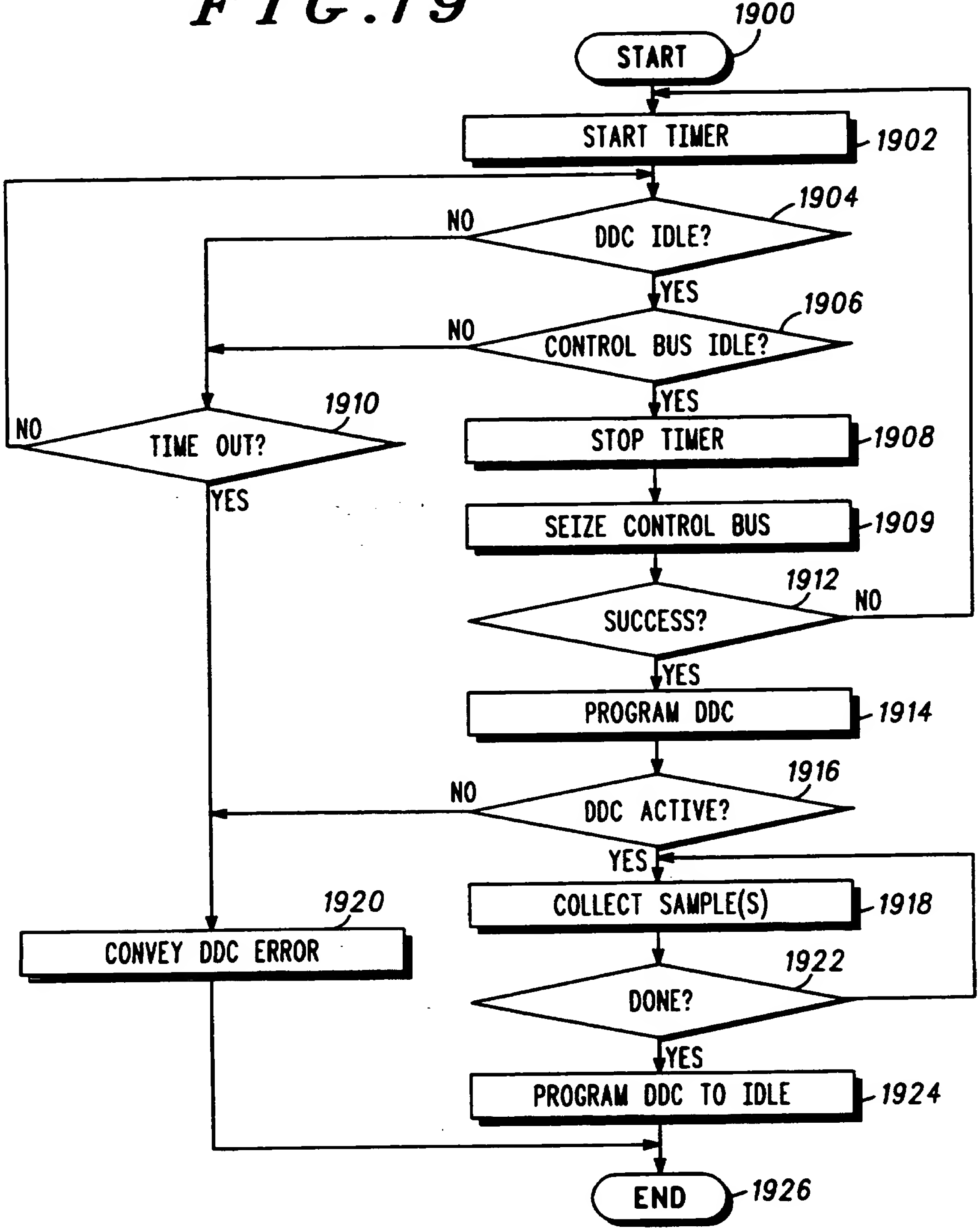

B/P I-O
1740
1806
DAC 1
1806
DAC 2
B/P I-O
1740'
CONTROLLER BLOCK
1748
"DUC" DIGITAL UP CONVERSION ASIC
1802
"DUC" DIGITAL UP CONVERSION ASIC
1802
CONTROLLER BLOCK
1748'
PROCESSOR
1742
PROCESSOR
1742'
MEMORY
1746
MEMORY
1746'
DSP
1744
DSP
1744'
PROCESSING FOR 4 CHANNELS
PROCESSING FOR 4 CHANNELS

FIG.18

FIG.19


1900
START
START TIMER
1902
1904
DDC IDLE?
NO
YES
1906
CONTROL BUS IDLE?
NO
YES
1910
TIME OUT?
NO
YES
STOP TIMER
1908
SEIZE CONTROL BUS
1909
1912
SUCCESS?
NO
YES
PROGRAM DDC
1914
1916
DDC ACTIVE?
NO
YES
COLLECT SAMPLE(S)
1918
1920
CONVEY DDC ERROR
1922
DONE?
YES
PROGRAM DDC TO IDLE
1924
END
1926

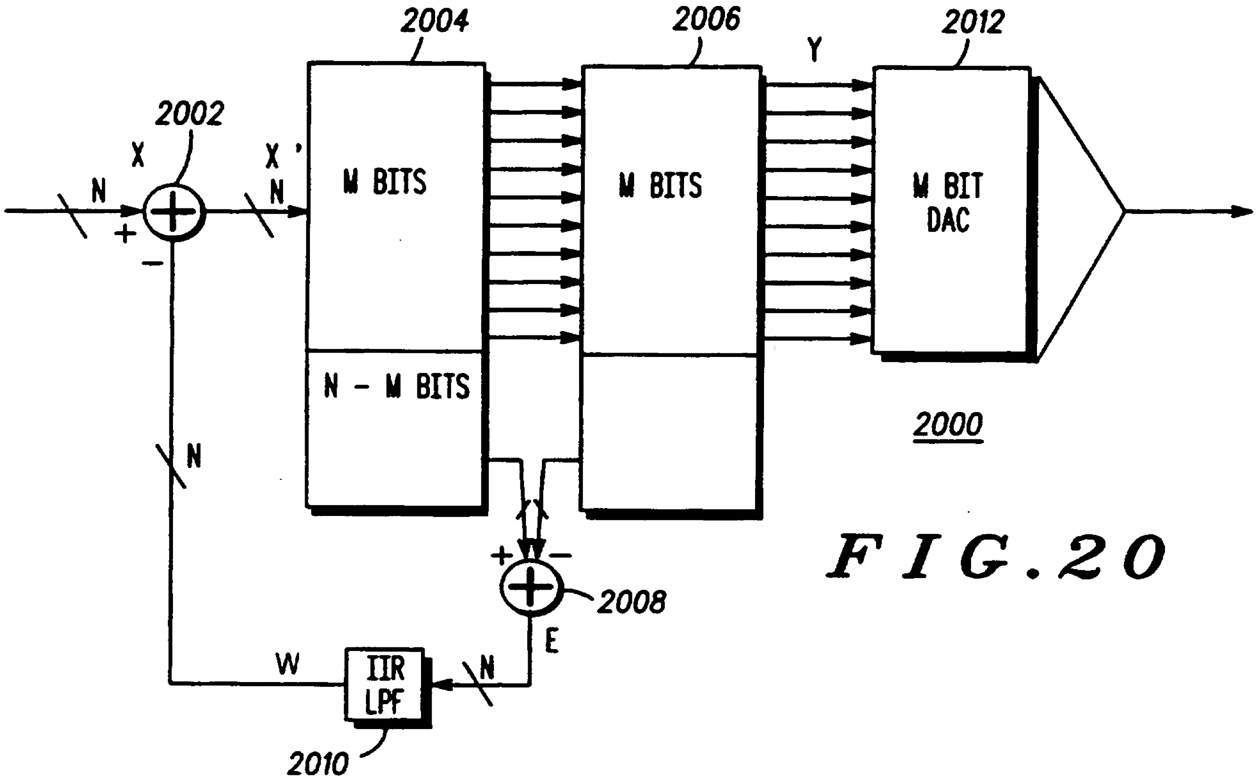
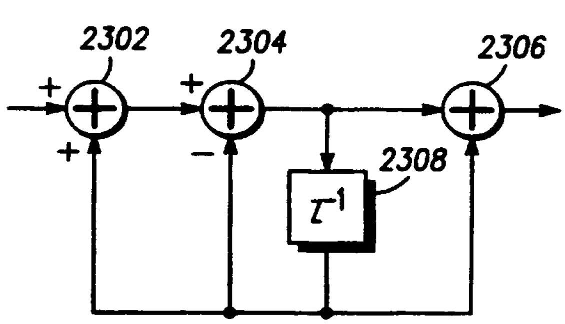

2004
2006
2012
Y
2002
X
X'
N
N
+
−
M BITS
M BITS
M BIT
DAC
N − M BITS
2000
N
+
−
2008
E
W
IIR
LPF
N
2010

FIG.20

FIG.21


2010
2302
2304
2306
+
+
+
−
2308
z^{-1}

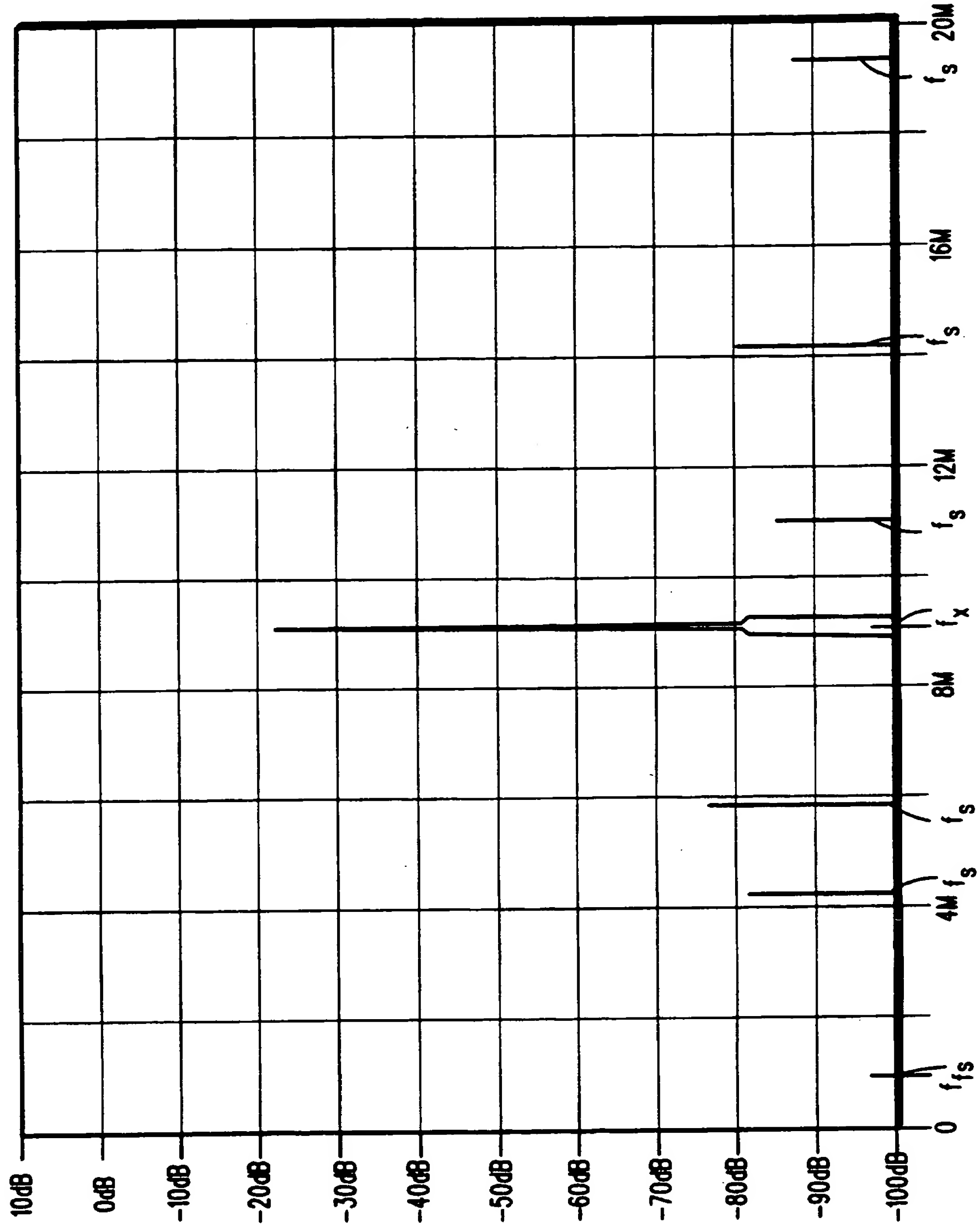

10dB
0dB
-10dB
-20dB
-30dB
-40dB
-50dB
-60dB
-70dB
-80dB
-90dB
-100dB
0
4M
8M
12M
16M
20M
f_s
f_x
f_{fs}

FIG. 22

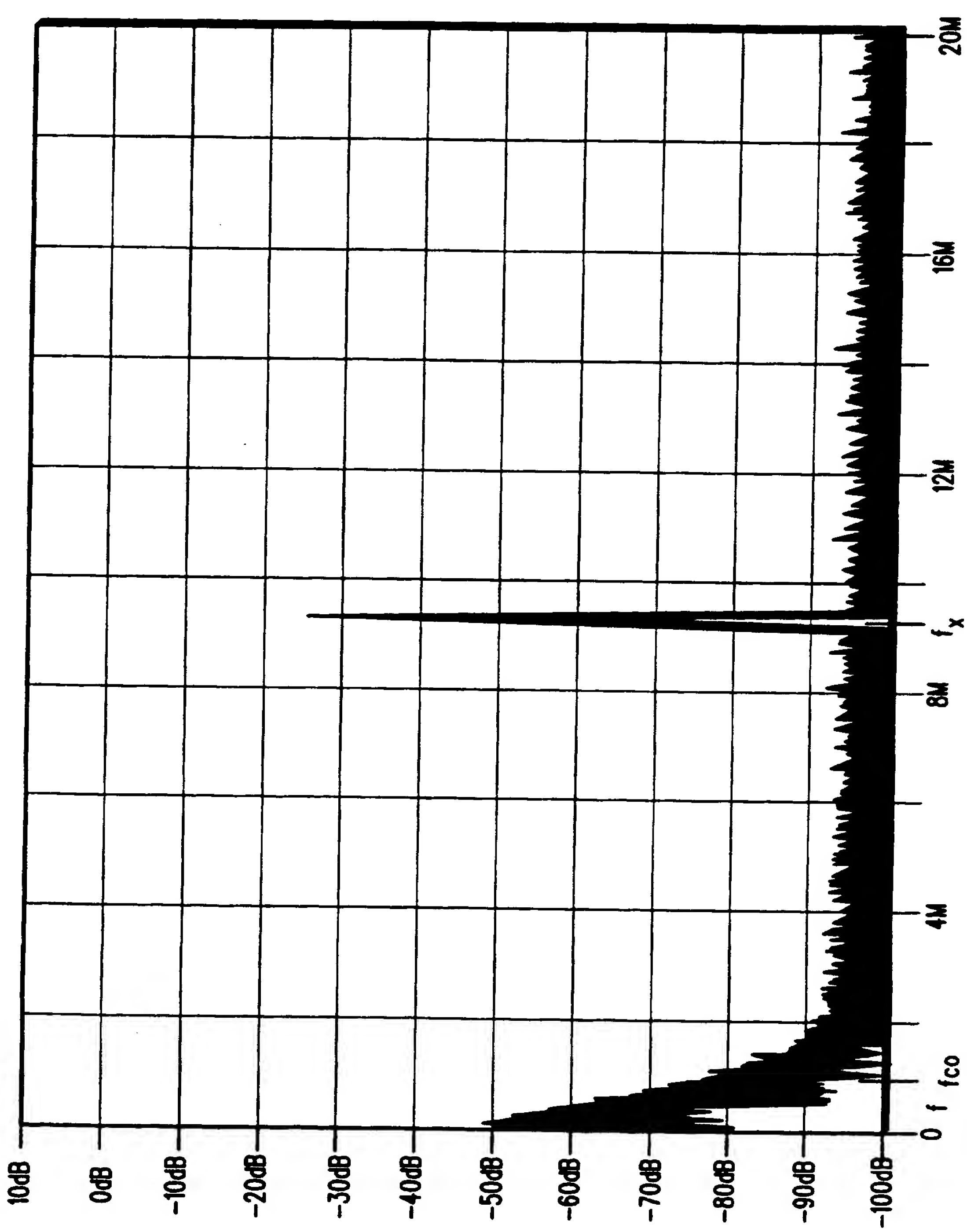

10dB
0dB
-10dB
-20dB
-30dB
-40dB
-50dB
-60dB
-70dB
-80dB
-90dB
-100dB
0
f
fco
4M
8M
f_x
12M
16M
20M

FIG. 23

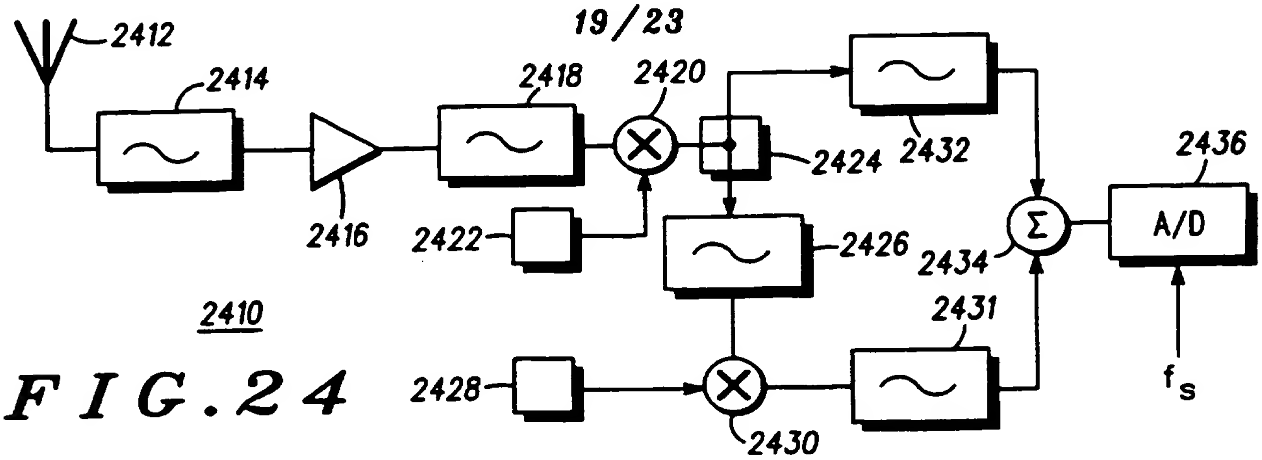


FIG. 24

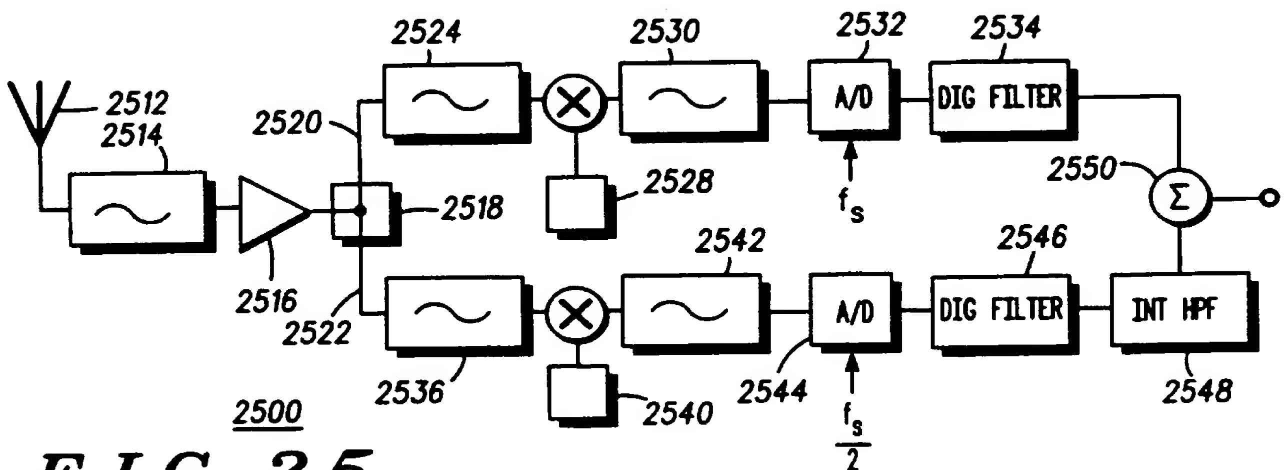


FIG. 25

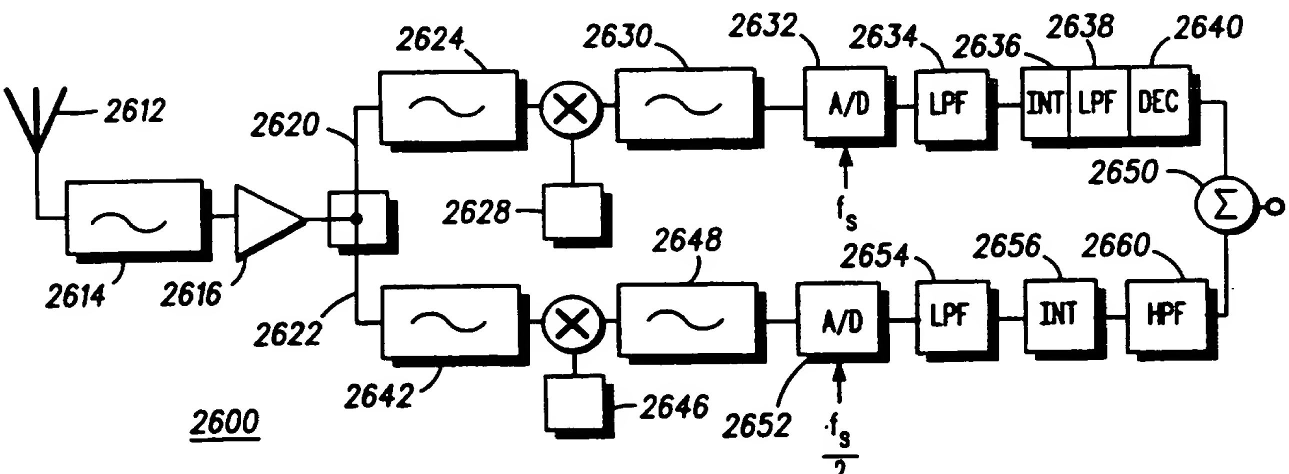


FIG. 26

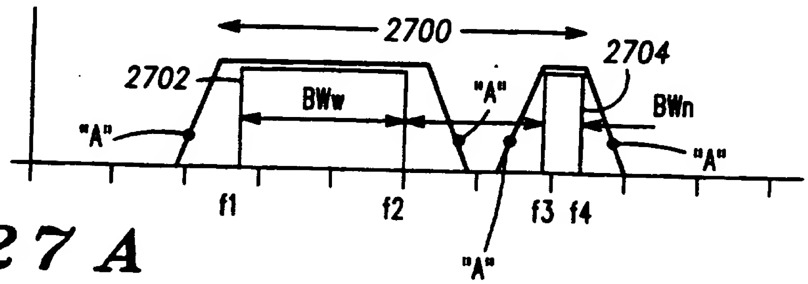


FIG.27A

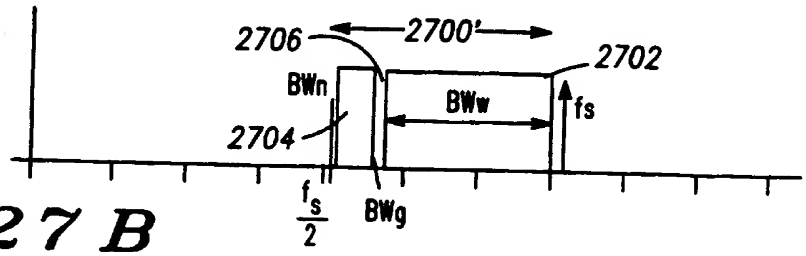


FIG.27B

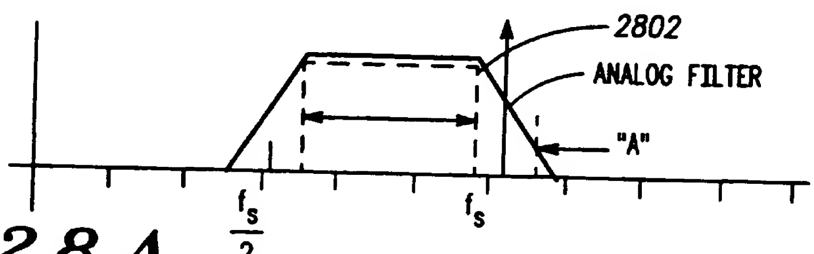


FIG.28A

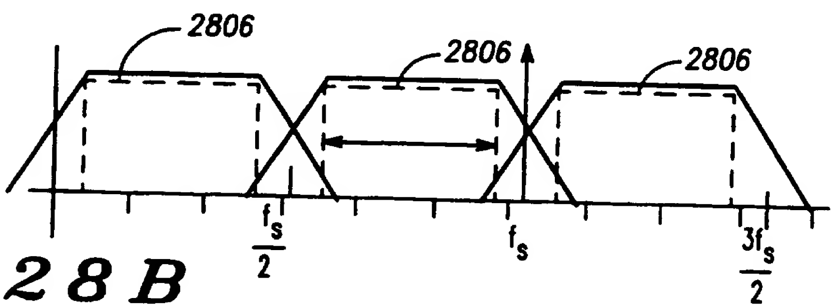


FIG.28B

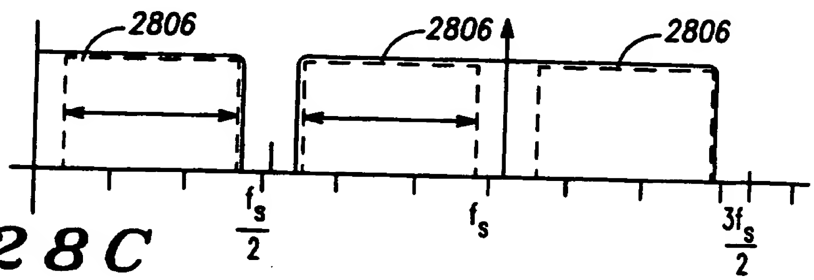


FIG.28C

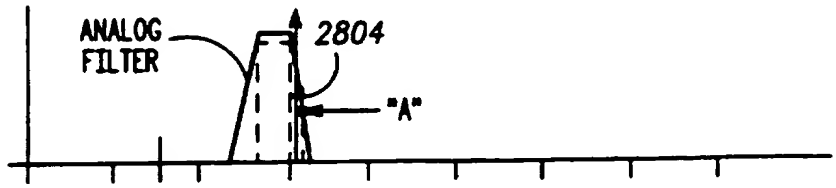


FIG. 28D

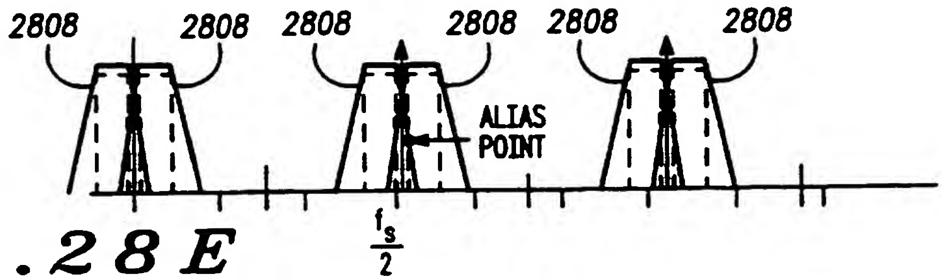


FIG. 28E

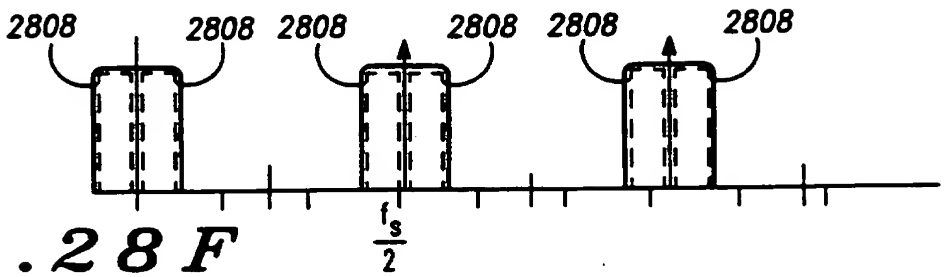


FIG. 28F

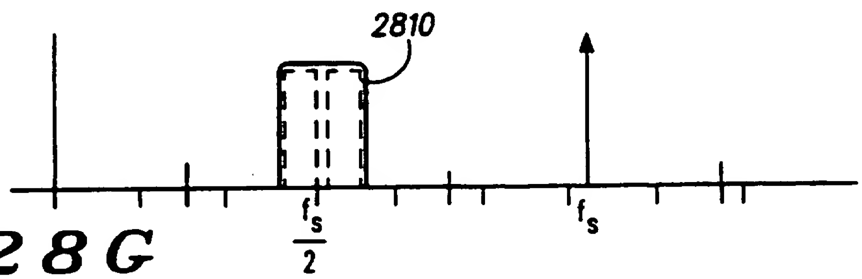


FIG. 28G

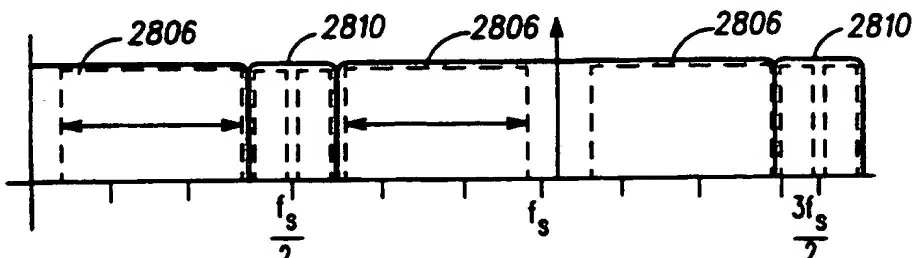


FIG. 28H

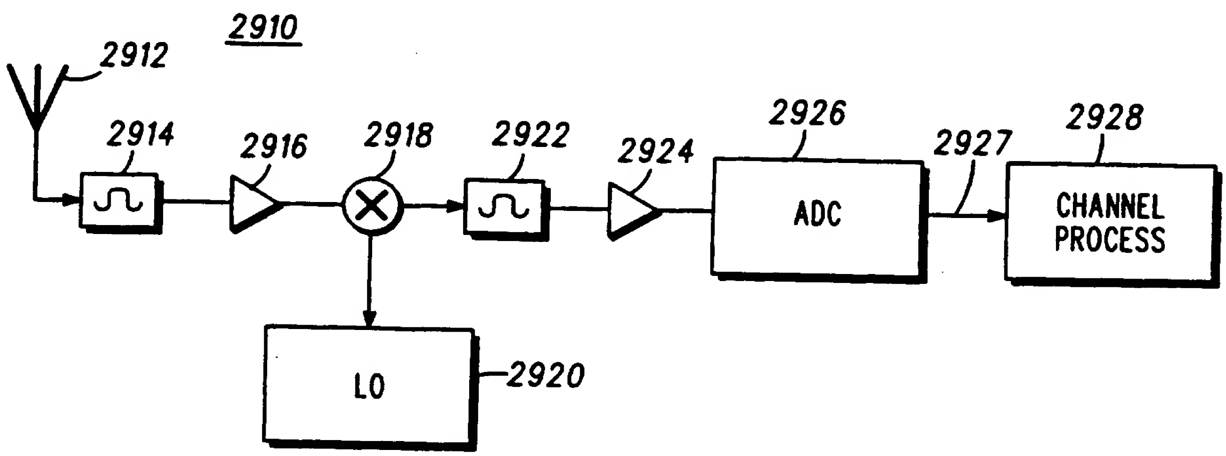

2910
2912
2914
2916
2918
2922
2924
2926
2927
2928
ADC
CHANNEL PROCESS
LO
2920

FIG.29

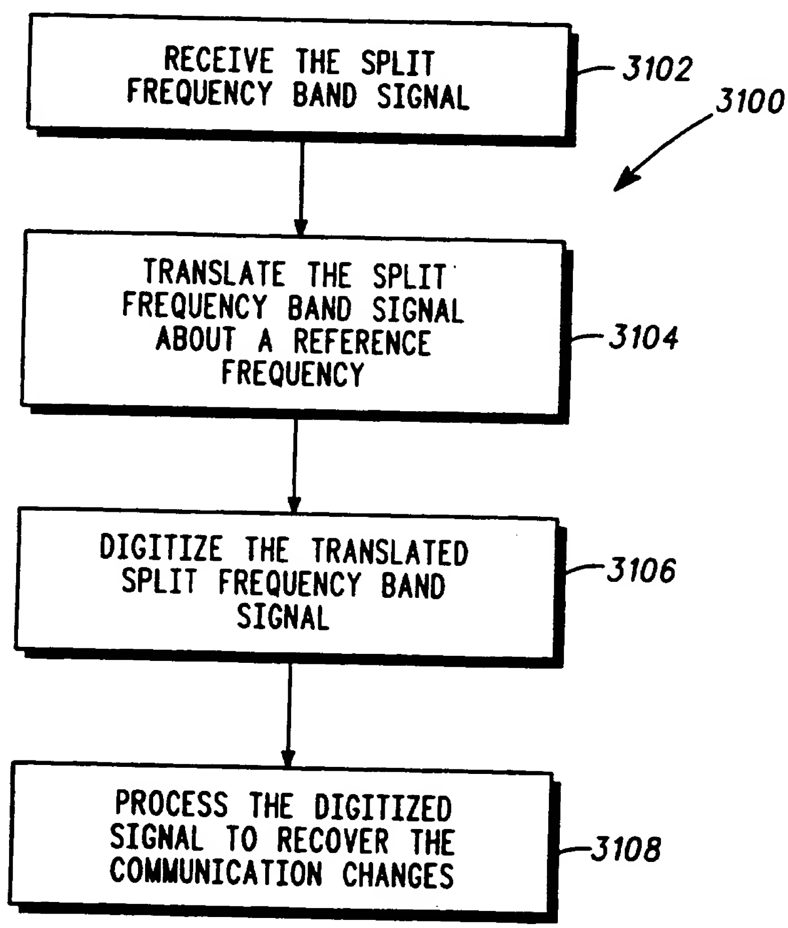

RECEIVE THE SPLIT FREQUENCY BAND SIGNAL
3102
3100
TRANSLATE THE SPLIT FREQUENCY BAND SIGNAL ABOUT A REFERENCE FREQUENCY
3104
DIGITIZE THE TRANSLATED SPLIT FREQUENCY BAND SIGNAL
3106
PROCESS THE DIGITIZED SIGNAL TO RECOVER THE COMMUNICATION CHANGES
3108

FIG.31

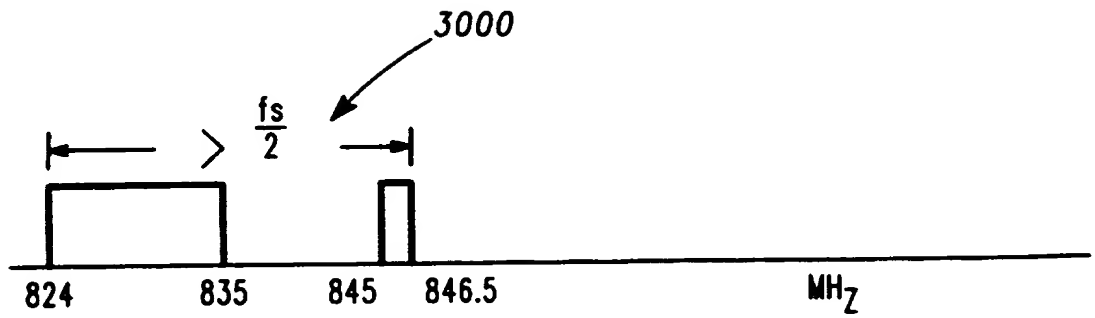


FIG.30A

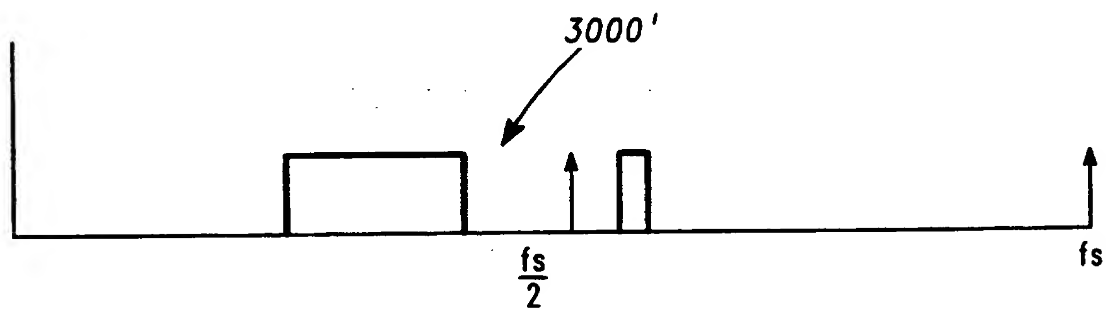


FIG.30B

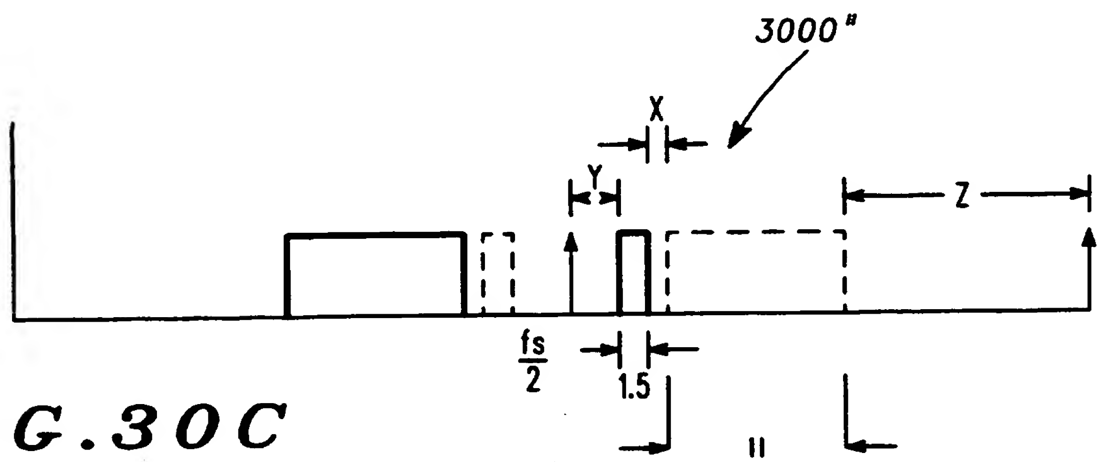


FIG.30C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/17014

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04L 27/06, 27/20
US CL :375/267, 299, 347; 455/101,103,132
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/200, 219-220, 259-260, 267, 299, 347, 350; 455/31.1, 33.3, 78, 84, 101,103,132-1333, 272, 277.1; 364/724.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US, A, 5,412,352 (GRAHAM) 02 May 1995, col. 3, line 59 to col. 4, line 17.	9
Y	US, A, 5,220,583 (SOLOMON) 15 June 1993, col. 2, lines 52-57.	1-3
Y	US, A, 3,783,385 (DUNN ET AL.) 01 January 1974, col. 4, lines 19-31.	1-3
A	US, A, 5,274,836 (LUX) 28 December 1993, col. 3, lines 12-55.	4-8
A	US, A, 4,616,364 (LEE) 07 October 1986, see Fig. 4.	1-3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be part of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 MARCH 1996	09 APR 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer YOUNG T. TSE
Facsimile No. (703) 305-3230	Telephone No. (703) 305-4736

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/17014

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Telephone Practice
Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest
☒ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

Group I, claims 1-8, drawing to a multi-channel transmitter and receiver, respectively.
Group II, claim 9, drawing to an upconverter/modulator within a digital transmitter.
The inventions listed as Group I and Group II do not meet the requirements for Unity of Invention for the following reasons:
The receiver in Group I is for receiving radio frequency signals, converting the radio frequency signals to IF digital signals, selecting one of the digital signals, and converting the digital signals to a baseband IF frequency signal; and the transmitter in Group I is for up converting and modulating a digital downlink signals to digital IF signals, summing sub-group of the digital IF signals, converting the digital IF signals to analog IF signals, upconverting the analog IF signals to radio frequency signals, and transmitting the radio frequency signals to an antenna. However, the upconverter/modulator within the digital transmitter in Group II specifically recites first and second selectors, first and second interpolation filters, first and second mixers, and an output adder. Although the transmitter of claim 4 in Group I recites a plurality of upconverters, no special technical feature of the upconverter was cited as the special technical feature of the upconverter/modulator of claim 9 in Group II. Therefore, the requirements of the upconverter recited in the transmitter of Group I do not correspond to the special technical feature of the upconverter/modulator within the transmitter of Group II.